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SPACECRAFT IF SWITCH MATRIX FOR ADVANCED TECHNOLOGY COMMUNICATION SATELLITE SYSTEMS

FINAL REPORT: PROOF-OF-CONCEPT MODEL

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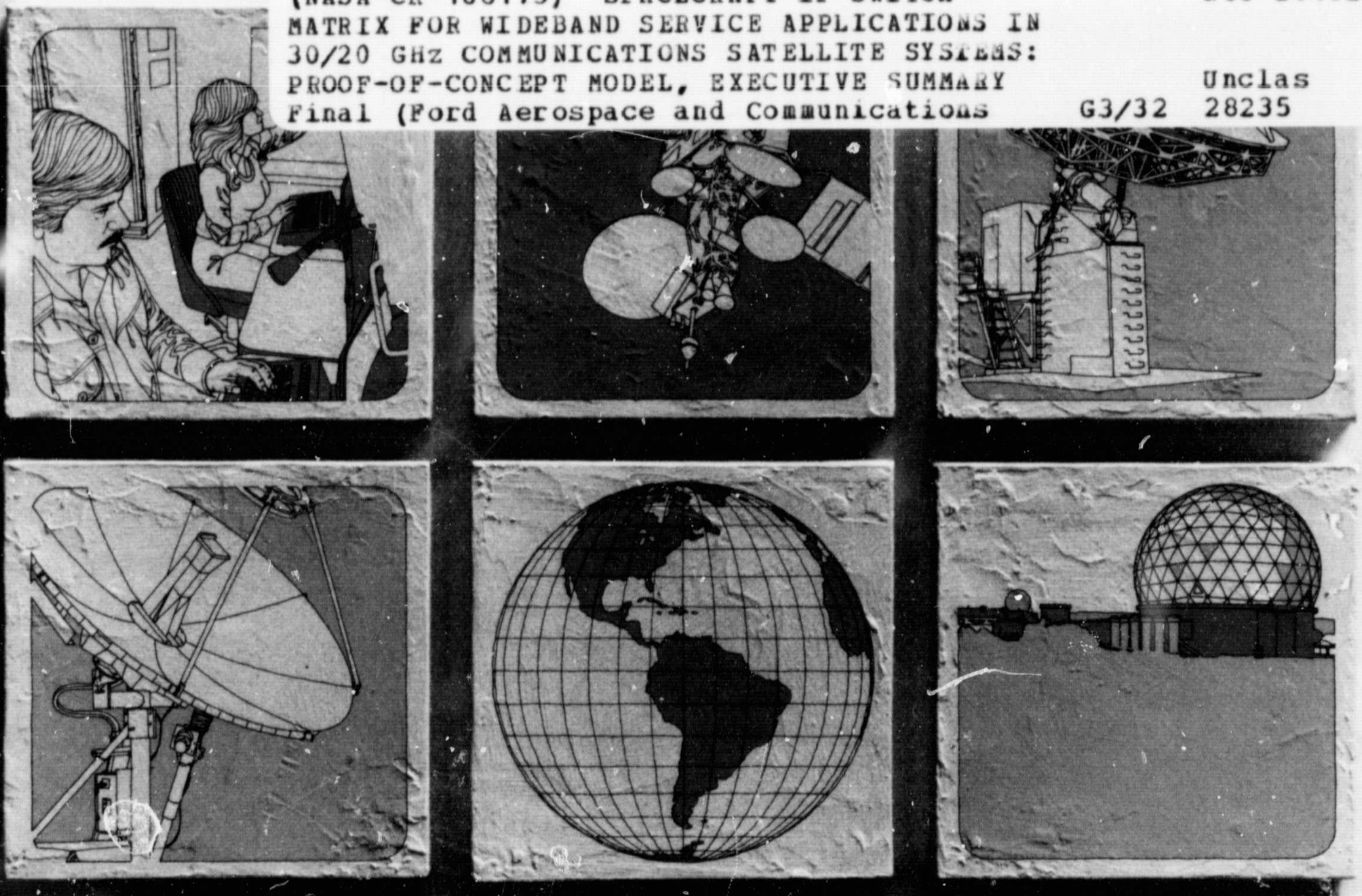

Ford Aerospace & Communications Corporation / Western Development Laboratories Division

NASA CR-168175

SPACECRAFT IF SWITCH MATRIX FOR WIDEBAND SERVICE APPLICATIONS IN 30/20 GHz COMMUNICATION SATELLITE SYSTEMS

EXECUTIVE SUMMARY

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16. Abstract

The use of a dynamic switching matrix for future communication satellites will significantly increase the communication channel capacity and improve the system capability and flexibility.

This report describes the design and development of a unique coupler crossbar 20 x 20 microwave switch matrix. This report presents the test results of the proof-of-concept model that meets the requirements for a high-speed satellite switched, time division multiple access (SS-TDMA) system.

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PREFACE

This Final Report on "Spacecraft IF Switch Matrix for Advanced Technology Communication Satellite Systems" describes the development effort performed by Ford Aerospace and Communications Corporation under Contract No. NAS3-22501 for NASA/Lewis Research Center.

The objective of this Final Report is to present the design, test data, and analysis of the 20 x 20 Proof-of-Concept Model Microwave Switch Matrix. The program was initiated on July 1,1980; and the Ford Aerospace program manager was Dr. P. Ho.

The technical staff contributing to this program included A. Anderson, E. Balderrama, N. Chiang, M. Chiang, E. Coban, E. Feng, K. Lee, J. Legg, J. Low, R. Malizewski, E. Molmen, J. Pelose, W. Spurgeon, and J. Wisniewski. This report was prepared by John Pelose and Eugene Coban. Special thanks goes to Ruby Schreck for her secretarial support throughout this program.

The NASA Technical Manager was E. W. Spisz.

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1.0 INTRODUCTION

Satellite-switched, time division, multiple access (SS-TDMA) is a key technology needed for future communication satellites. SS-TDMA is an effective method of significantly increasing communication satellite channel capacity and improving communication satellite system flexibility.

For the SS-TDMA system, an IF switch matrix is required on the spacecraft to provide interconnectivity among the multiple beam antennas. The system will require signal processing on-board the satellite.

The development of microwave switch matrices to be used in multiple-beam antenna systems and communication systems requiring dynamic interconnectivity among the beams is a key technology item. System studies have identified switch matrices as a major factor in achieving minimum cost and efficient use of frequency and orbital resources.

The major task of the development of the proof-of-concept (POC) 20 x 20 switch matrix was to demonstrate the feasibility of a system providing high capacity channel interconnectivity on board a 30/20 GHz multiple beam communication satellite for a flight qualifiable switch matrix.

This switch matrix will provide 2.5 GHz band width in the frequency band from 3.5 GHz to 6.0 GHz with a switching speed of less than 10 ns.

Figure 1.1 shows the functional configuration of an SS-TDMA transponder equipped with a 20 x 20 switch matrix. The transponder system includes the IF switch matrix with control unit, which provides signal routing between the uplink and downlink spot beam antennas for trunking

SS-TDMA TRANSPONDERS

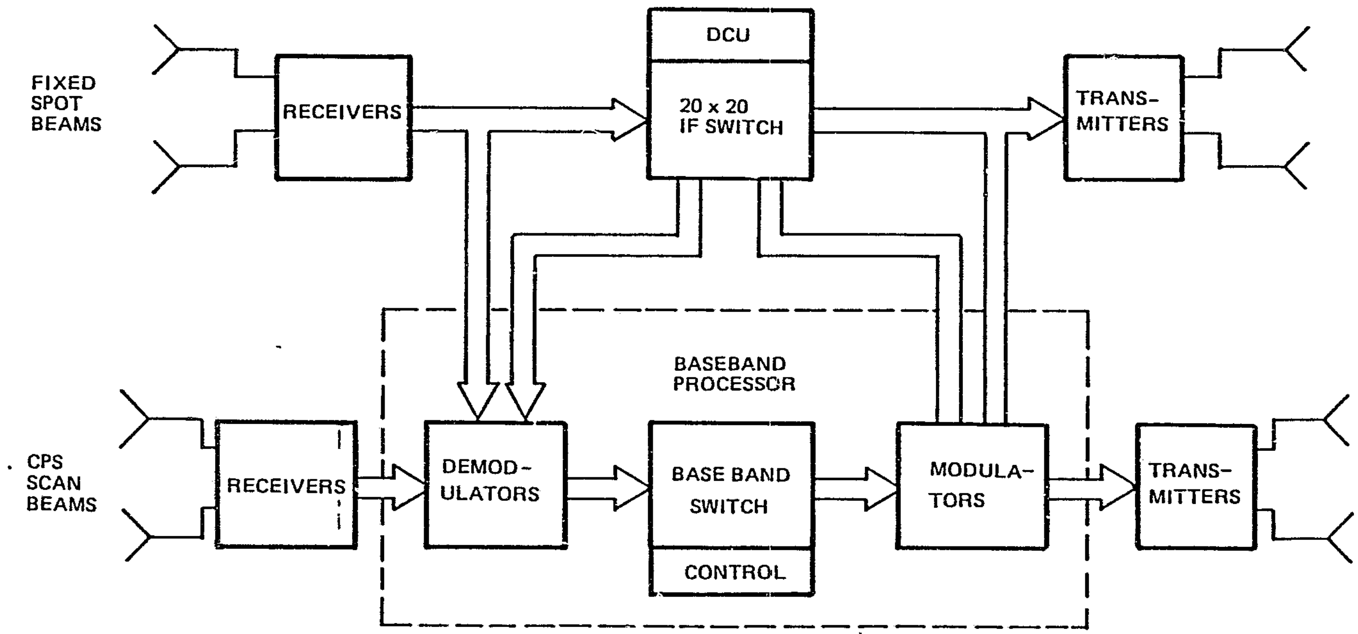

Fig. 1.1

applications and a baseband switch and a demodulator for the scanning beam service.

The uplink signals from spot beam antennas are first down converted to a common IF and then routed via the IF matrix switch to the designated transmitters for upconversion and retransmission.

Several different types of switch matrix systems have been developed and reported using different architectures. The architecture selected for POC development herein provides many functional capabilities including the broadcast mode and the variable switching time capability. The broadcast mode (one input signal connected to multiple outputs simultaneously) is advantageous for SS-TDMA system synchronization. The variable switching time capability (turn on and turn off any crosspoints for any desired duration) provides for a higher communication efficiency. The distribution control algorithm determines the complexity of the digital control circuitry. The selected coupler crossbar architecture uses a planar mechanical structure which improves the switch RF performance, reliability, manufacturability and minimizes weight, size and power consumption.

Figure 1.2 shows how a time division multiple access system can provide high speed dynamic interconnectivity between three transmitting/ receiving earth terminals .

The main tasks of this two-year program were to analyze the design concepts for large or medium size switch matrices, assess the present and future technology, develop a proof-of-concept (POC) model using available technology and fabricate a highly versatile switch matrix

SATELLITE-SWITCHED TIME DIVISION MULTIPLE ACCESS
(SS-TDMA)

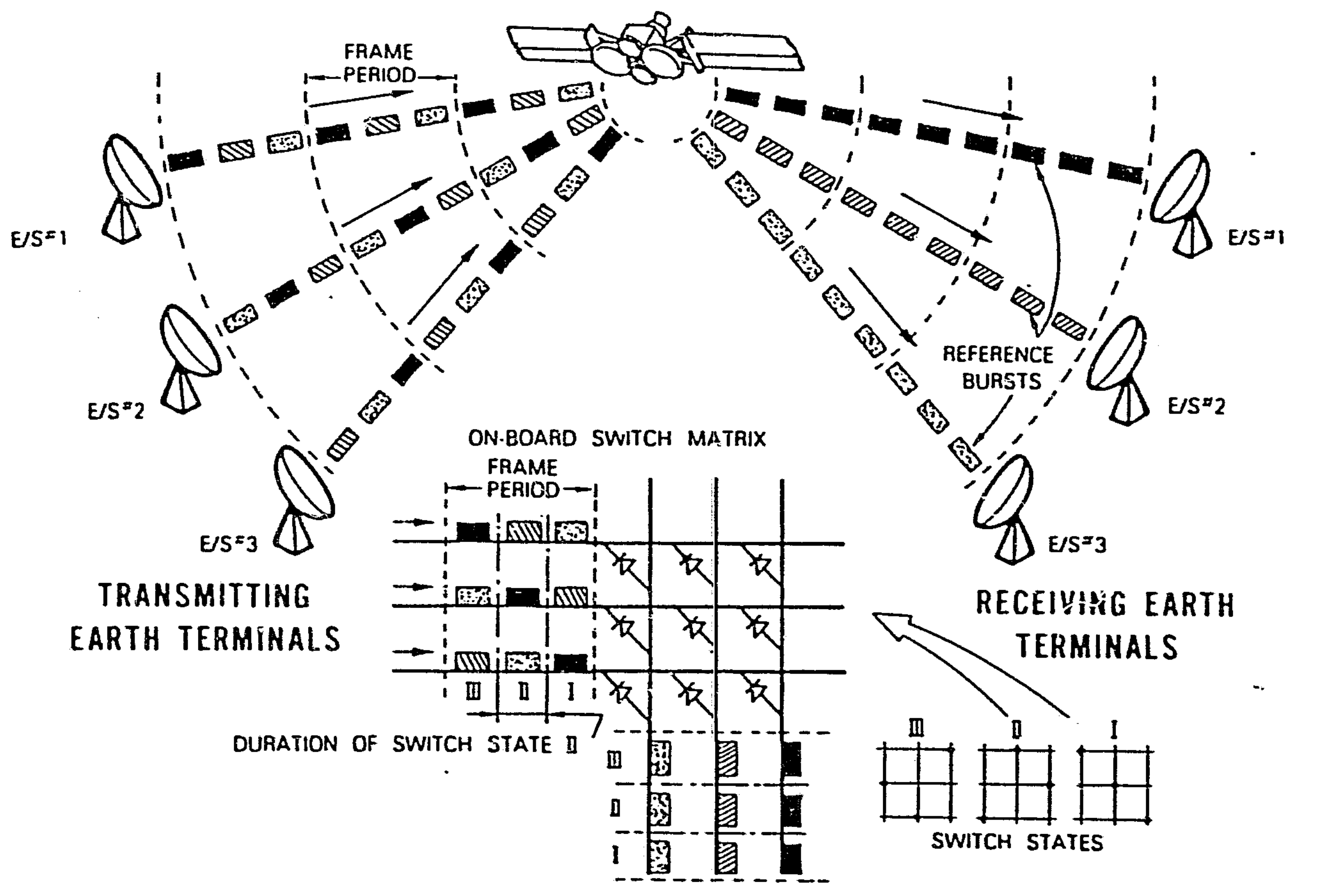

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Fig. 1.2

system, with low power consumption, small size, low weight, and good reliability characteristics.

The contractual effort focused upon the system architecture design, analysis, detailed design, and fabrication. The main deliverable item was the proof-of-concept model suitable for demonstrating TDMA channel interconnectivity in a multibeam communications system.

2.0 PROGRAM OBJECTIVES AND REQUIREMENTS

The main objective of the switch matrix program was the assessment of available switch matrix technology suitable for the development of advanced communication satellites for SS-TDMA applications and provides a strong base by accomplishing the following:

a. Technology evaluation for microwave switch matrix (MSM)

b. Conceptual matrix architecture design and analysis

c. Detail component design and analysis

d. Fabrication and test of Proof-of-Concept (POC) model

e. Reliability analysis for MSM

f. Recommendations for future development and fabrication.

The objectives include the hardware development of a complete switch matrix system consisting of the microwave switch matrix, the distribution control unit, and the associated special testing equipment.

The primary intent and the underlying philosophy of the IF Switch Matrix development effort were to verify the readiness of the technology required to implement dynamic routing of traffic on-board high capacity multibeam communication satellites and to demonstrate not only the

technology readiness of functional and electrical performance, but also reliability and redundancy.

The concept of the multibeam satellite system which can utilize the IF Switch Matrix is shown in Figure 1.1. The constraints, specifications and goals to which the IF Switch Matrix POC Model was designed and built are as follows:

a. General

The POC IF Switch Matrix System shall demonstrate the high-speed switching characteristics for the dynamic interconnectivity between 20 input and 20 output ports on board a multibeam communication satellite operating in a TDMA mode.

The Switch Matrix will operate in the IF frequency region between 3 to 8 GHz and will consist of the switching elements and related signal circuitry, the switch drivers, and the appropriate control and decoding network required to address the desired switching elements.

It was assumed that an on-board computer processor would provide the control signals to the IF Switch Matrix in order to establish the required switch configuration and durations as shown in Figure 1.1. However, in order to demonstrate system operation, it was necessary to design and provide as special testing equipment a suitable control unit to operate the system in a dynamic manner.

b. Matrix Size

The IF switch matrix was designed to accommodate 20 input and 20

output ports. The matrix size is referred to as 20 x 20 and was designed to incorporate the corresponding 400 crosspoints (switching elements). The POC model, however was only partially populated. The control and decoding circuitry, however, was designed to handle all 400 crosspoints.

c. Reliability

High reliability was a major concern in the POC model design. The POC model was designed to maintain full connectivity for 10 years. Redundancy to handle switching element failure was included as a feature of the design.

d. Redundancy

In the case of crosspoint switch failure, redundancy was incorporated into the matrix architecture by including additional "wraparound" rows and columns to provide alternate signal paths.

e. Advanced Technology Concepts

The IF Switch Matrix was designed to utilize advanced technology components which would be available in the 1983 and 1987 time period.

f. Space Qualifiable Components

Only potentially space qualifiable components and materials were used for the design. All fabrication and packaging techniques were selected to provide a space qualifiable design. The design minimized value, weight and power dissipation.

The PCC IF Switch Matrix System was built using space qualifiable generic components and materials.

g. Expandability to Larger Systems

The POC IF Switch Matrix System was designed so that it could be scaled to larger matrix sizes with the corresponding increase in the size, weight, and DC power consumption.

h. Environmental Design Objectives

The IF Switch Matrix was designed to withstand those mechanical electromagnetic, thermal, vacuum, and radiation stresses to be incurred during the prelaunch handling, shuttle ascent and deployment, perigee and apogee stage firings and long term (10 year) operation in synchronous orbit environments.

i. Workmanship

A high workmanship quality was maintained to ensure product integrity and assurance.

j. Repairability

During the manufacturing and test phases a disciplined system of failure reporting, effect analysis and corrective action was used. The IF Switch Matrix System was developed for repairablity with using spare interchangeable modules and subassemblies.

k. Expected Performances of POC IF Switch Matrix Model

Table 1.1 presents the contract specifications and the design goals of the POC IF Switch Matrix Model. In this table, the outline dimensions, weight and other mechanical characteristics of the POC model are presented. The DC power consumption and reliability are also estimated. The design approach emphasized minimum power, volume and weight.

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TABLE 1.1

CONTRACT SPECIFICATONS AND DESIGN GOALS OF THE

PROPOSED 20 X 20 POC MODEL IF SWITCH MATRIX

PARAMETERS	CONTRACT REQUIREMENTS	DESIGN GOALS EXPECTED PERFORMANCE
Matrix Size	20 x 20	20 x 20 with 12 active inputs and 8 outputs
POC Connectivity	400 active crosspoints (Redundancy included)	
Reconfiguration Rate	2 microseconds	1 microsecond to 1 ms
Switching Time	10 nanoseconds	10 ns (10% to 90%)
IF Frequency	3 to 8 GHz (center)	3.5 to 6.00 GHz
IF Bandwidth	1000 MHz (min)	2500 MHz (goal) 1000 MHz (min)
Insertion Loss	18.0 dB (Max)	18.0 dB (Max)
Gain/Loss Ripple	1.0 dB per 1000 MHz	1.0 dB per 1000 MHz
Phase Linearity Variation	+/-5 degrees over BW	+/-5 degrees over BW
Isolation	40.0 dB (Min)	40.0 dB (min)
Input VSWR	1.5/1.0	1.5/1.0
Output VSWR	1.20/1.0	1.5/1.0
Input Signal Level	-30 dBm to -10 dBm	-30 dBm to -10 dBm
1-dB Compression Point	N/A	-10 dBm at the input
Max. Input Signal Level	+ 10 dBm	+ 10 dBm CW
Noise Level (below output level)	35 dB	35 dB
DC Input Power Total DC Input Power	N/A	40.0 watts

3.0 MAJOR TASKS AND PROGRAM ACCOMPLISHMENTS

3.1 Task 1. IF Switch Matrix Design Using 1982 Technology

During Task I, the basic design with tradeoff studies was completed for the microwave switch matrix. The technology assessment identified that the basic architecture consisting of a coupler cross—bar switch matrix was most suitable and could be implemented with present technology.

An analysis was performed and the basic coupler crossbar architecture, with redundancy, offered trade-off advantages between matrix size, functional performances, reliability, etc. The results of the Task 1 were summarized in the Interim Task 1 Report (Document WDL-TR8968) and in the Task 1 Final Report (Document NASA #1-5-F-1-T1). These reports served as the basis for the design of the 20 x 20 POC model.

The studies of the POC model defined the functional block diagrams for the switch matrix and distribution control unit, developed the methods of circuit integration, and selected the frequency band for minimum interferences with optimum functional performance and specifications.

The study revealed the following advantages of coupler crossbar matrix architecture:

- Planar structure with possible monolithic MIC in the future.
- Modular approach with simple manufacturing.
- Enhanced reliability due to:
  - Minimum active devices per crosspoint
  - Failure of a device resulted in, at the most, the loss of only one crosspoint
  - Redundancy is simplier to implement
- Good input/output match
- Input/output signal level independent on the switching path
- Broadcast mode of operation with no input matching degradation

A comparison coupler crossbar switch matrix functional capabilities are illustrated in Table 3.1.1.

Table 3.1.1

FUNCTIONAL CAPABILITIES OF MICROWAVE SWITCH MATRIX ARCHITECTURES

Architecture	Fan-out/ Fan-In	Single-pole- Multiple-	Rearrange- able Switch	Coupler Crossbar
Broadcast Mode	Yes	No	No	Yes
Variable Time Assignment	Yes	Yes	No	Yes
Mechanical	Cubic	Cubic	Planar	Planar

The four matrix architecture concepts are illustrated in Figs. 3.1.1 through 3.1.4.

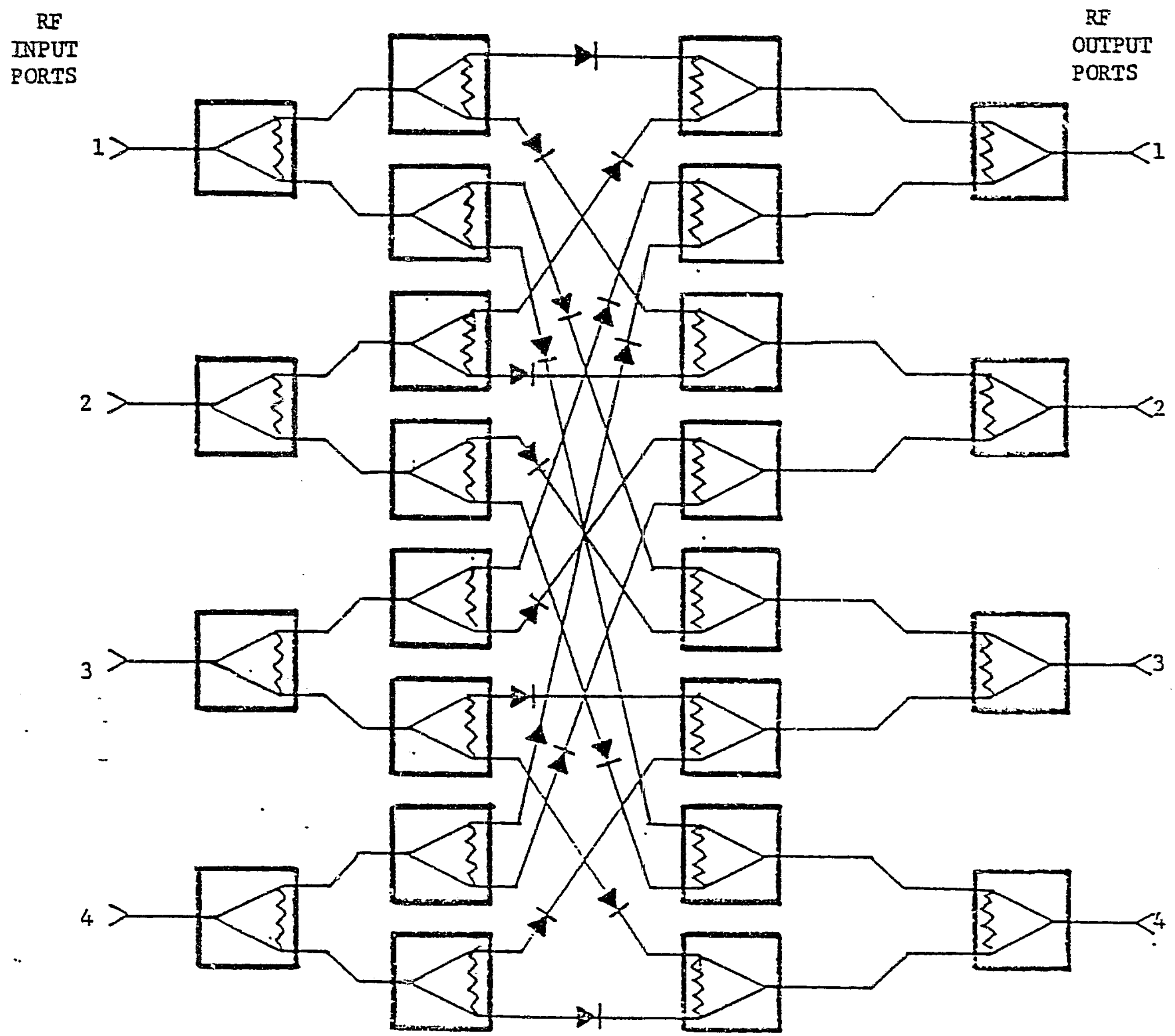

Fig. 3.1.1 POWER DIVIDER FAN-OUT/FAN-IN SWITCH MATRIX ARCHITECTURE CONCEPT

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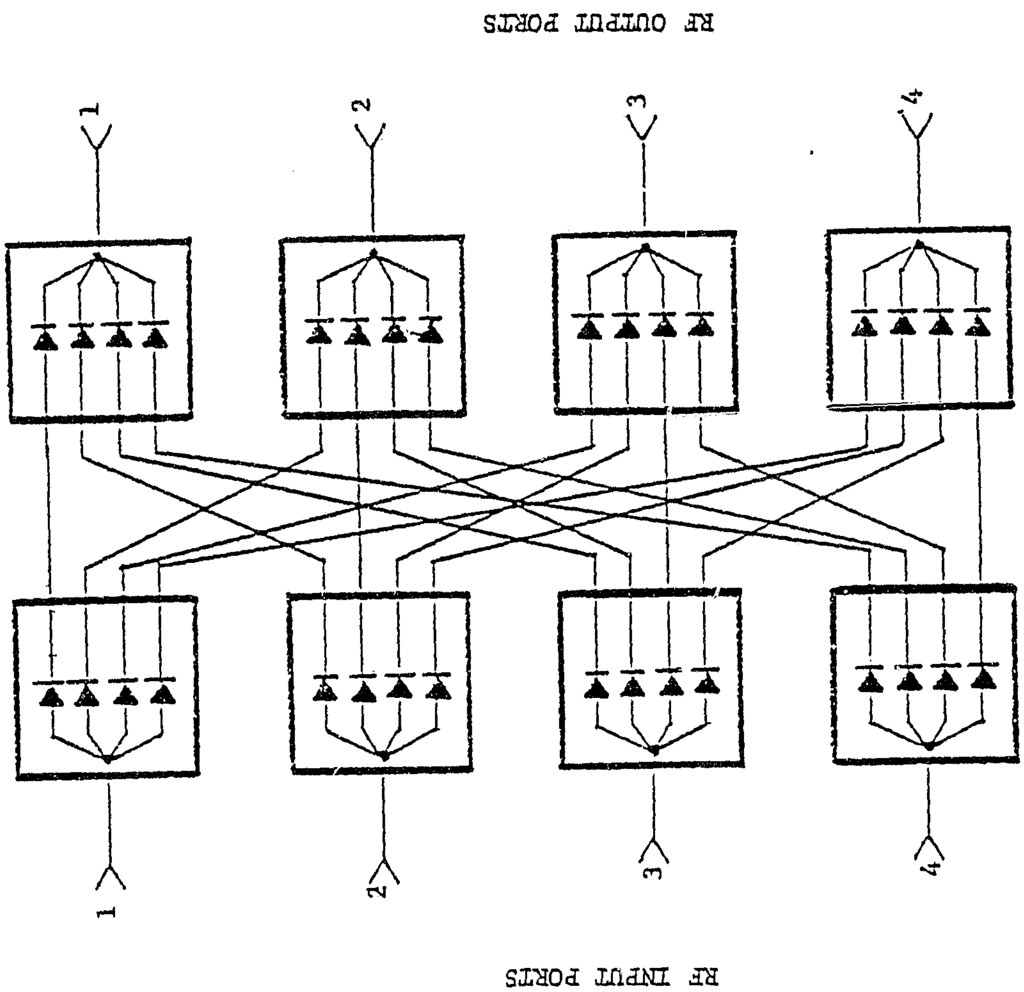
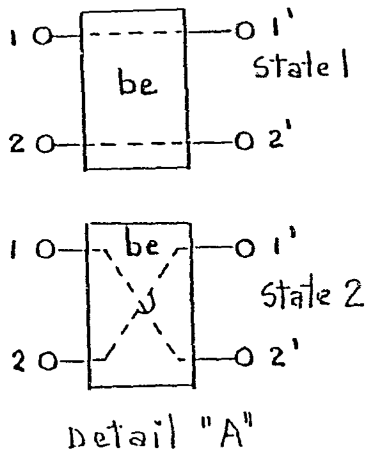


Fig. 3.1.2 SINGLE-POLE-MULTIPLE-THROW (SPMT) SWITCH MATRIX ARCHITECTURE CONCEPT



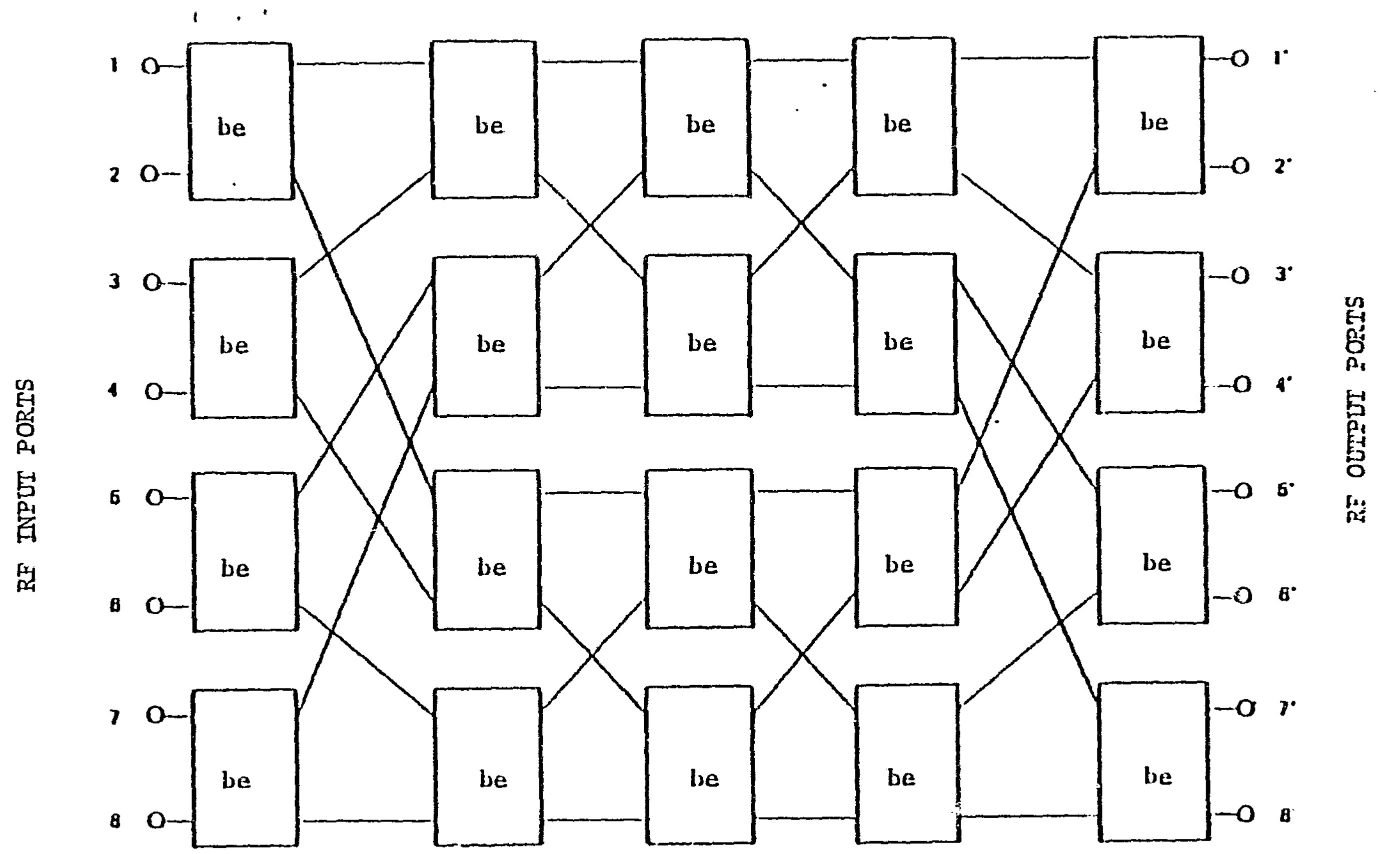


Fig. 3.1.3 REARRANGEABLE SWITCH MATRIX ARCHITECTURE CONCEPT

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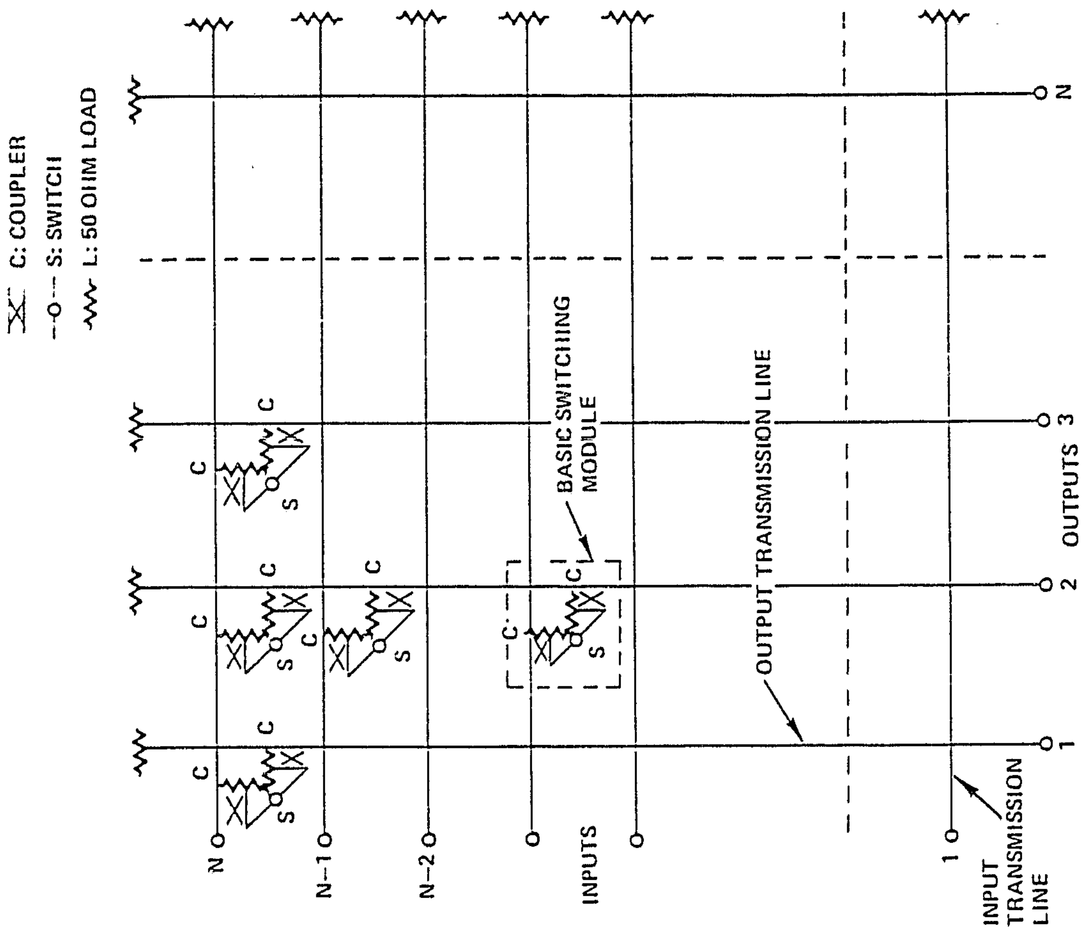

Fig. 3.1.4 COUPLER CROSSBAR SWITCH MATRIX ARCHITECTURE CONCEPT

The application of the dual-gate GaAs FET as the switching device in the microwave switch matrix was selected due to the following advantages:

- Low insertion loss due to switching device gain.
- High isolation
- Low driver power
- High switching speed
- Suitability for monolithic integration

A major review of the Task 1 results was conducted at NASA/Lewis Cleveland on February 2, 1981. That presentation also included the large RF and baseband switch matrix concepts and the design approach for a 4 x 4 breadboard switch matrix using 1981 technology.

3.2 Task 2. Alternate Switch Matrix Design Using 1987 Technology

A large (100 x 100) switch matrix and a large (100 x 100) baseband switch matrix were analyzed based on the technology that was forecast to be available before 1987. It was projected that by using 1982 switch matrix architecture combined with the future technology of LSI/VLSI circuits and monolithic microwave integrated circuits (MMIC) already in advanced state of development, that a 100 x 100 switch matrix could be realized.

The results of the study were presented in the final Task 2 report (Document NASA 1-11-F1-T2) and were directed toward configurations which could include new device concepts for large matrices. The final design concept, presented in the report, included a description of switch architecture and controlling circuits, functional description,

reliability prediction and specifications, and identified these technologies that must be developed for a 100 x 100 or larger microwave or baseband matrix.

The final conclusions showed that an integrated version of a 100 x 100 microwave switch matrix with roughly equivalent characteristics as the 20 x 20 MSM could be developed using 1987 technology. The 100 x 100 switch matrix presents reduced weight, size and DC power consumption. The recommended matrix design consisted of one hundred 10 x 10 MMIC submodules. Such an integrated 100 x 100 switch matrix could weigh only 15 lb. A similar matrix built using 1982 technology would weigh a few hundred pounds. The volume of the integrated 100 x 100 switch matrix with 10000 crosspoints is 72 cubic inches in comparison with the 520 cubic inches of the 1982 design for a 20 x 20 switch matrix (with 400 crosspoints only).

3.3 Task 3. Breadboard Development of Critical Switch Technology

The intent of the Task 3 breadboard development effort was to devise solutions for critical technology items identified in Task 1. The main high speed circuits and modules for the switch matrix and the DCU were designed, tested and integrated into a 4 x 4 breadboard microwave switch matrix unit.

The 4 x 4 unit was fully populated with 16 crosspoints and was fabricated and tested at the Ford Aerospace and Communications Corporation and is presented in Figs. 3.3.1 and 3.3.2.

Fig. 3.3.1 shows the top view of the 4 x 4 breadboard matrix with 8 switch-driver modules. The bottom view presented in Fig. 3.3.2 shows

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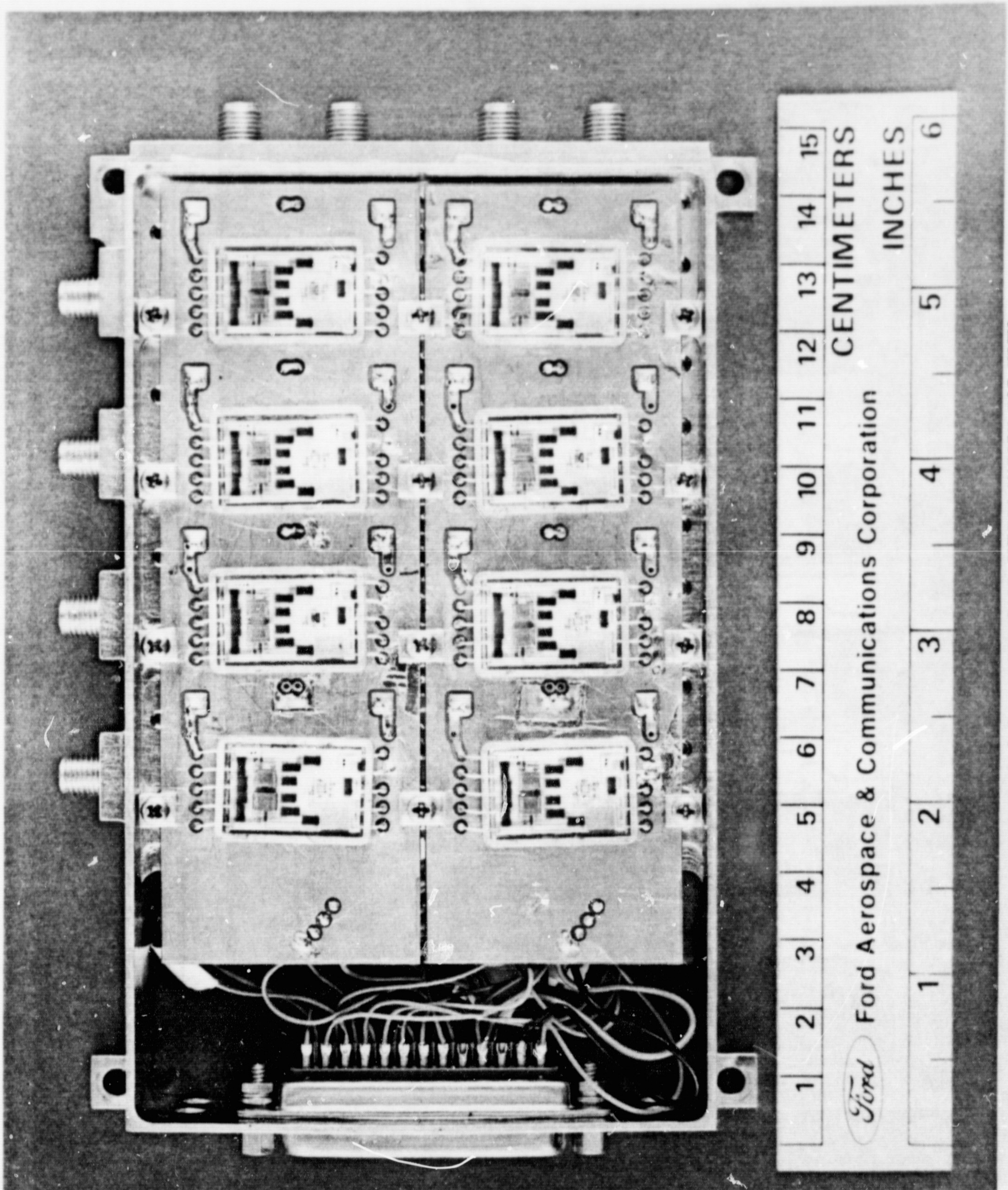

FIGURE 3.3.1 BREADBOARD SWITCH MATRIX TOP VIEW

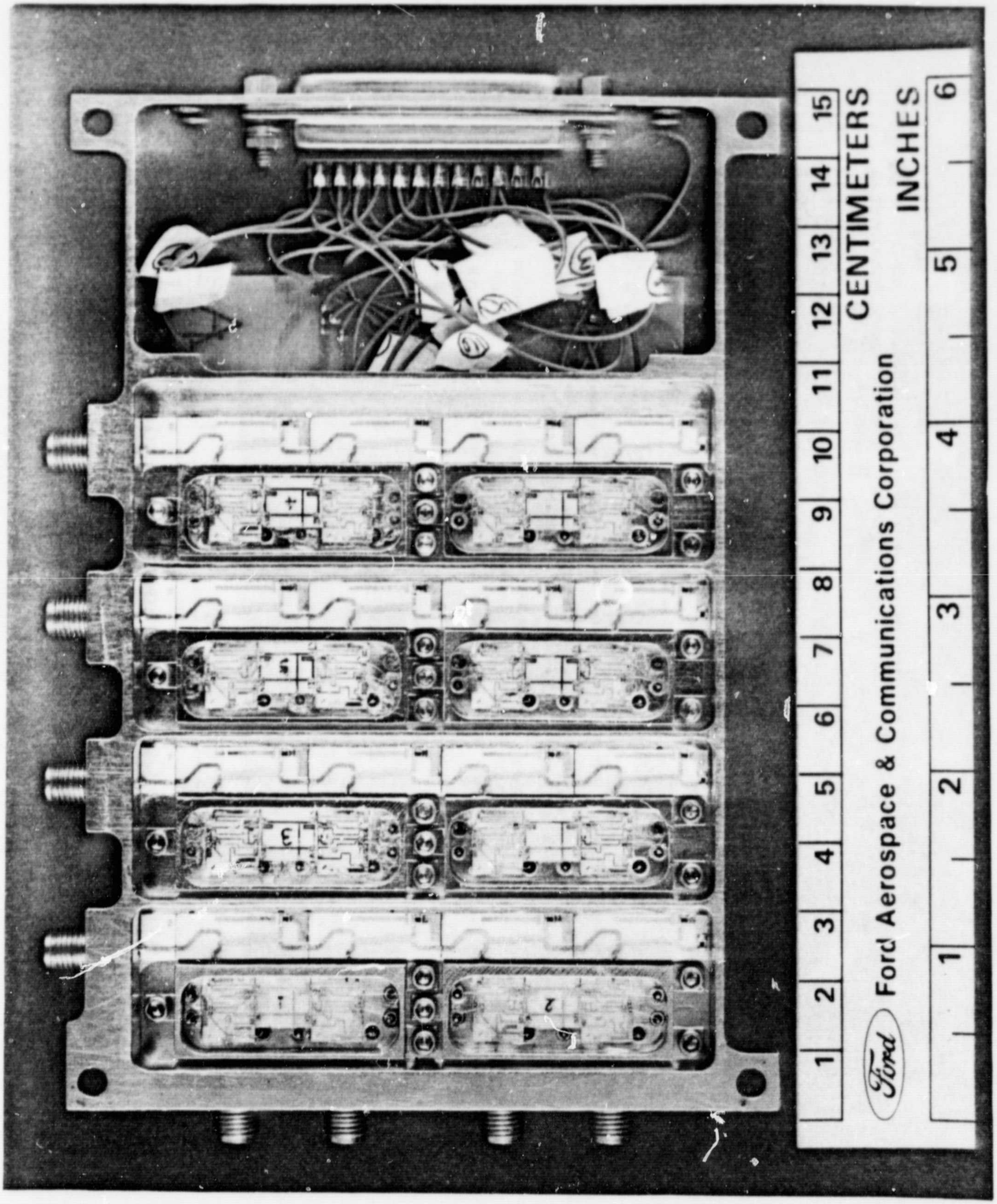

FIGURE 3.3.2 BREADBOARD IF SWITCH MATRIX BOTTOM VIEW

the interdigitated couplers and 8 dual crosspoint modules.

The distribution control unit for the 4 x 4 breadboard unit is presented in Fig. 3.3.3. The fully operational 4 x 4 matrix was tested and the results are presented in Table 3.3.1. The experience gained during the integration of that system and the encouraging results obtained in testing the breadboard model was used as the basis for the design and development of the 20 x 20 POC model, which is a more complex switch matrix system with improved performance.

The results of the breadboard development effort were presented in the Task 3 Final Report NASA 2-4-F1-T3.

3.4 Task 4. POC Model Planning and Specifications

A detailed development plan for the switch matrix along with specifications, was generated during the Task 4 study. The outputs of this task were presented at a minor review in which the following documents were reviewed and/or updated before starting the POC model design, fabrication, and testing:

1. Development Plan
2. Design and Performance Specifications
3. Interface Specifications
4. Top Level Proof-of-Concept Test Plan

3.5 Task 5. POC Model Design, Test Plan and Test Equipment

The actual design of the POC model hardware, including the detailed POC test plan and special test equipment design, were performed during Task

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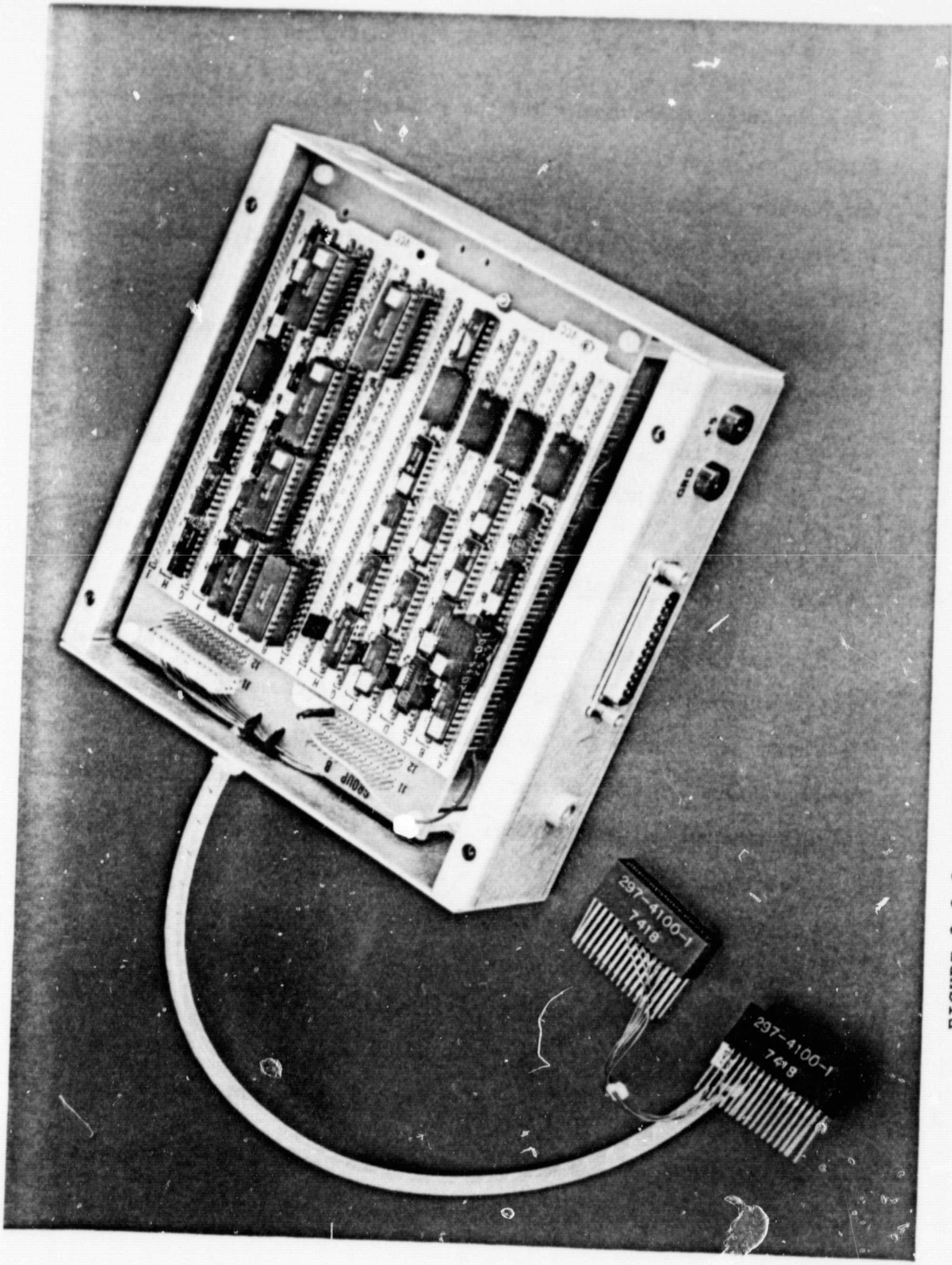

FIGURE 3.3.3 DISTRIBUTION CONTROL UNIT FOR 4 x 4 MSM

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Table 3.3.1

4 x 4 IF SWITCH MATRIX

BREADBOARD TEST DATA SUMMARY

Matrix Size:		4 x 4	
No. of Active Crosspoints:		16	
Connectivity:		Any input to any output and Broadcast Mode	
Reconfiguration Rate:		1 us	
Switching Time	ON:	50 ns (see Note)	
	OFF:	12 ns	
Center Frequency:		4.0 GHz	
Bandwidth @ 1 dB end points:		> 750 MHz	
Insertion Loss/Gain "ON":		Mean	3.92 dB
		Standard Deviation	0.66 dB
Group Delay: (3.5 to 4.5 GHz)		Mean	0.960 ns
		St. Dev.	0.340 ns
Input VSWR	"ON":	Mean	1.26:1
		St. Dev.	0.13
	"OFF":	Mean	1.24:1
		St. Dev.	0.10
Output VSWR:	"ON"	Mean	1.24:1
		St. Dev.	0.11
	"OFF"	Mean	1.19:1
		St. Dev.	0.11
1-dB Compression Point: (TYP)		Input:	-2 dBm
		Output*	-1 dBm
Isolation:		Mean	59.0 dB
		St. Dev.	3.7 dB
DC Power Consumption: (Switch matrix only)		2.9 Watts	

ote: *) Switching time less than 10 nsec is achieved with lower capacitance value at second gate of FET switch.

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V. The fundamental design concept was based on the results and experience obtained during the 4 x 4 breadboard switch matrix integration and testing.

In a meeting held on November 18, 1981 at NASA/Lewis Research Center, test data were presented to demonstrate that the 20 x 20 POC model would be capable of meeting the specifications. Thermal and functional performance were analyzed and an outline and packaging concept for the 20 x 20 POC matrix were presented. The outline drawing of the 20 x 20 POC model is presented in Figure 3.5.1.

The installation of the feedthrus laterally on the module housing simplifies the assembly and integration of the switch matrix. The bandwidth goal for the POC model was increased from 1000 MHz (minimum, in the specification) to 2500 MHz, with only a minor compromise in terms of increased insertion loss and input/output VSWR. The design of the proof-of-concept model was the result of a careful technology assessment in which the microwave switching circuits and switch driver circuits had been individually breadboarded and tested.

The main switching circuit (referred to as the switch amplifier module) uses dual-gate GaAs FETs operating in a gain mode as the switching element. GaAs FETs have demonstrated the capability of high switching speed and excellent isolation in the "OFF" state. The switching speed of the matrix is mainly limited by the response of the associated switch-driver circuit; the switching speed of the GaAs FET is on the order of 0.1 ns.

The switch-driver circuit supplying the control voltage to the second

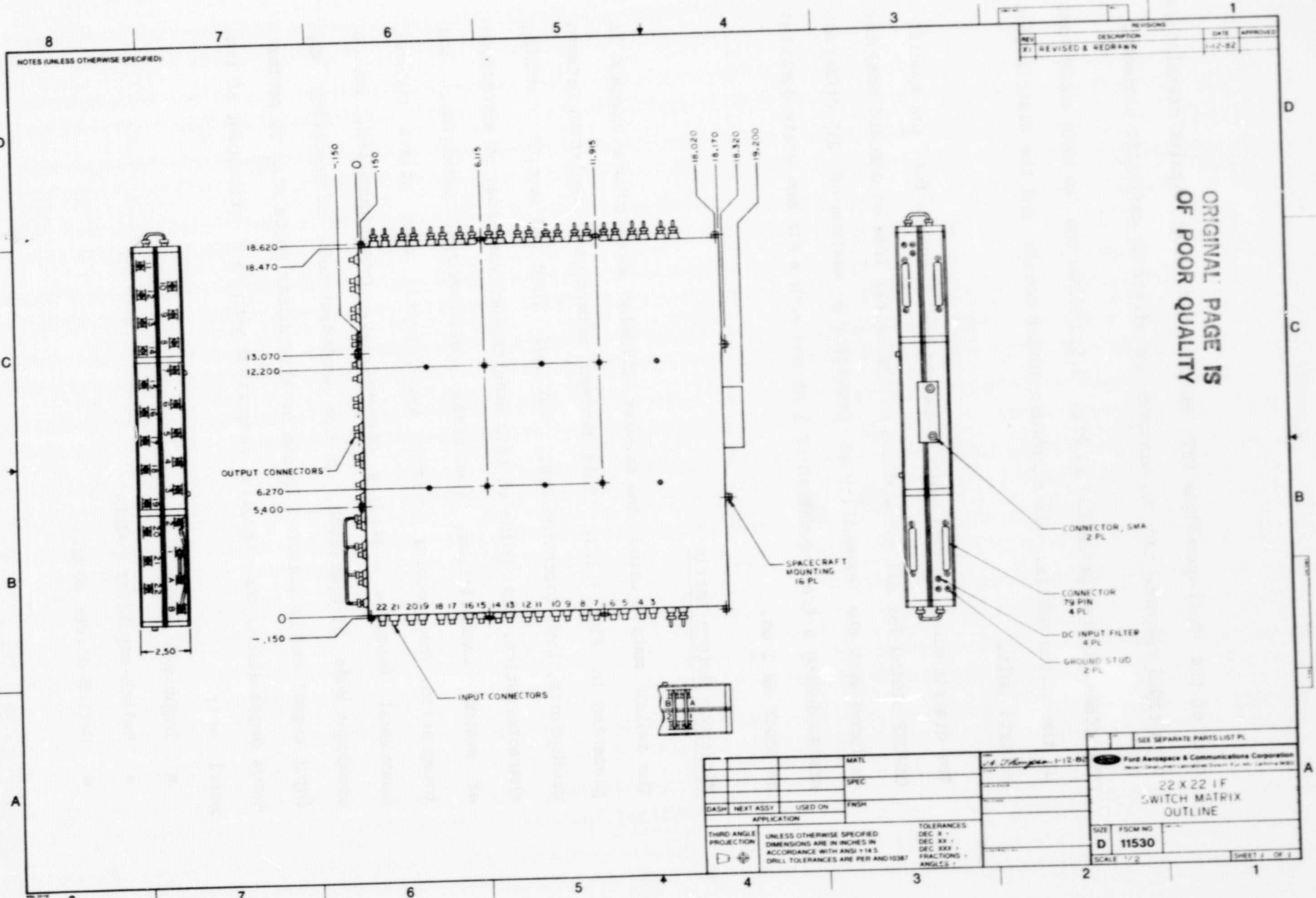

FIGURE 3.5.1 22 x 22 MSM OUTLINE

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gate of the dual-gate GaAs FET was designed using bipolar transistors with rapid response time to minimize the effect of parasitic elements.

The block diagram presented in Fig. 3.5.2 shows the two main subsystems of the switch matrix, the microwave switch matrix and the distribution control unit.

The distribution control unit receives the commands for the specific ON/OFF states for all crosspoints of the matrix from an onboard computer designed with the capability of providing a maximum of 256 different states during a frame duration of 1 ms and with a minimum state duration as short as 1 us.

a. Microwave Switch Matrix

The switch matrix using the coupler crossbar architecture concept is presented in Fig. 3.5.3. This concept offers good isolation between crosspoints, low insertion loss, and good input and output matching characteristics. The choice of this architecture was based on advantages of system capabilities, electrical performances, packaging, and integration. The coupler crossbar switch matrix also offers special functional features regarding connectivity, reconfiguration, and a broadcast mode of operation. In the broadcast mode of operation any input signal can be switched to one or all outputs ports with no performance degradation. The circuits associated with each crosspoint of the matrix are:

- Input and output directional couplers
- Switch-amplifier module
- Switch-driver module

IF SWITCH MATRIX SYSTEM

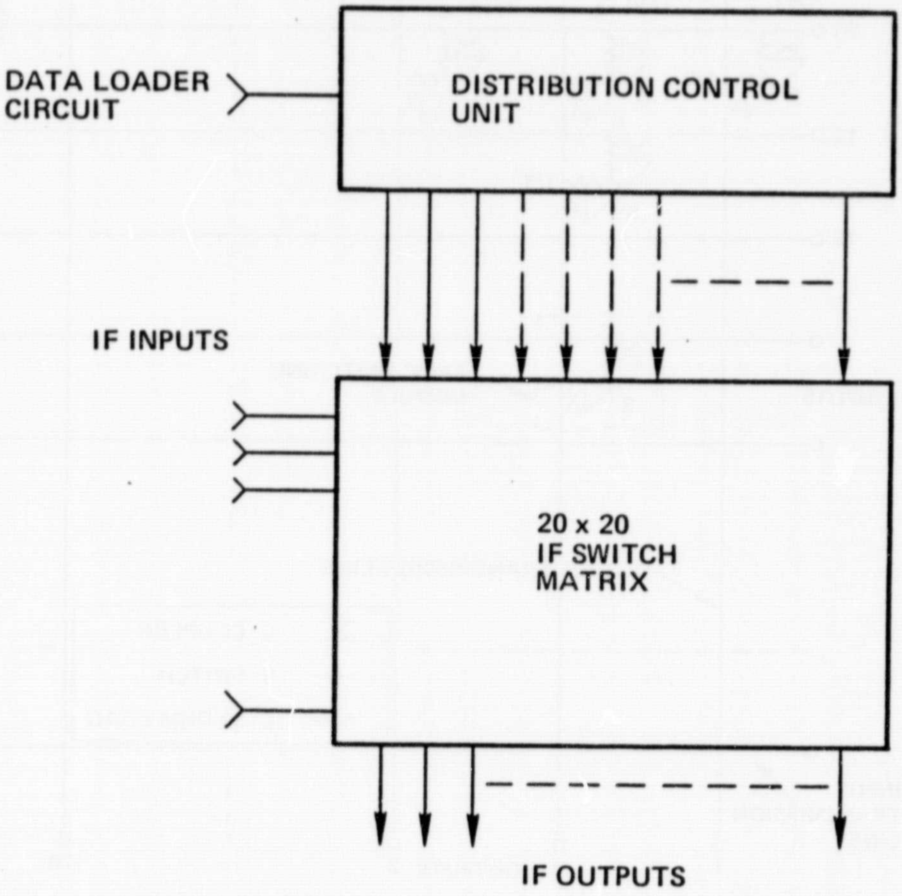

Fig. 3.5.2

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20 X 20 IF SWITCH MATRIX
USING COUPLER CROSSBAR ARCHITECTURE

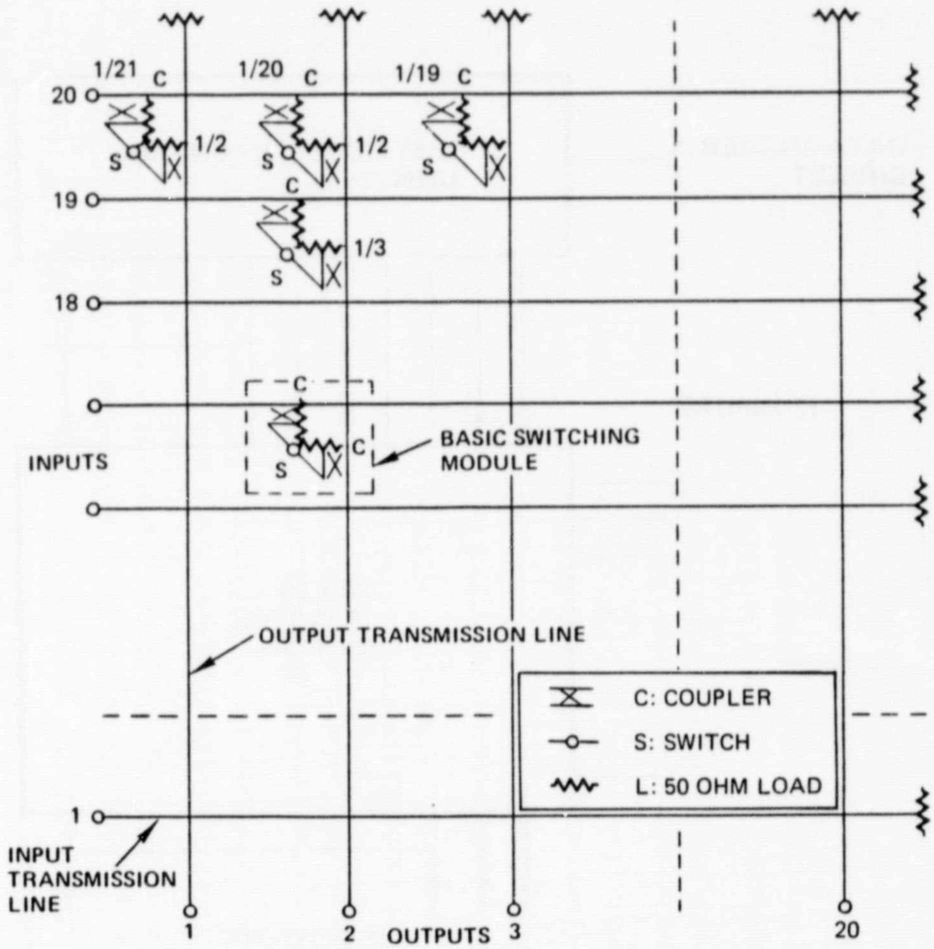

Fig. 3.5.3

Directional couplers with different coupling coefficients are used to connect the input lines of the matrix with the crosspoint switch amplifier module of the matrix. The coupling coefficients are selected so that the RF power level available at the ouput port of the input couplers is constant regardless of crosspoint location. After switching and amplification, the RF signal is fed to the desired output port of the matrix through the output directional coupler. The coupling coefficients of the input/output directional couplers depend on the crosspoint location in the matrix, and are selected such that the insertion loss is constant and independent of the signal path. The insertion loss of the input and output couplers is partially compensated for by the gain in the switch-amplifier. The relation between the coupling coefficients, K_n and K_{n+1} of two adjacent couplers on the same row or column of the matrix is given by:

$$1/K_{n+1}=1/(K_n+1)$$

Assuming the coupling coefficient of the last coupler is 1/3, the coupling coefficients of the next couplers will be 1/4, 1/5, and so on, depending on the matrix size. The actual coupling coefficients of the input and output couplers must also account for losses along the microstrip transmission lines.

The design of the two-stage switch-amplifier circuit was based upon the characterization and evaluation of several dual-gate FETs. The circuit is conceptually shown in Figure 3.5.4. The FET device chosen for the microwave switch amplifier is the Raytheon RDX-832 DGFET in chip form. This device provides good electrical performance while providing ease of handling and assembly. From the measured S-parameter characteristics of

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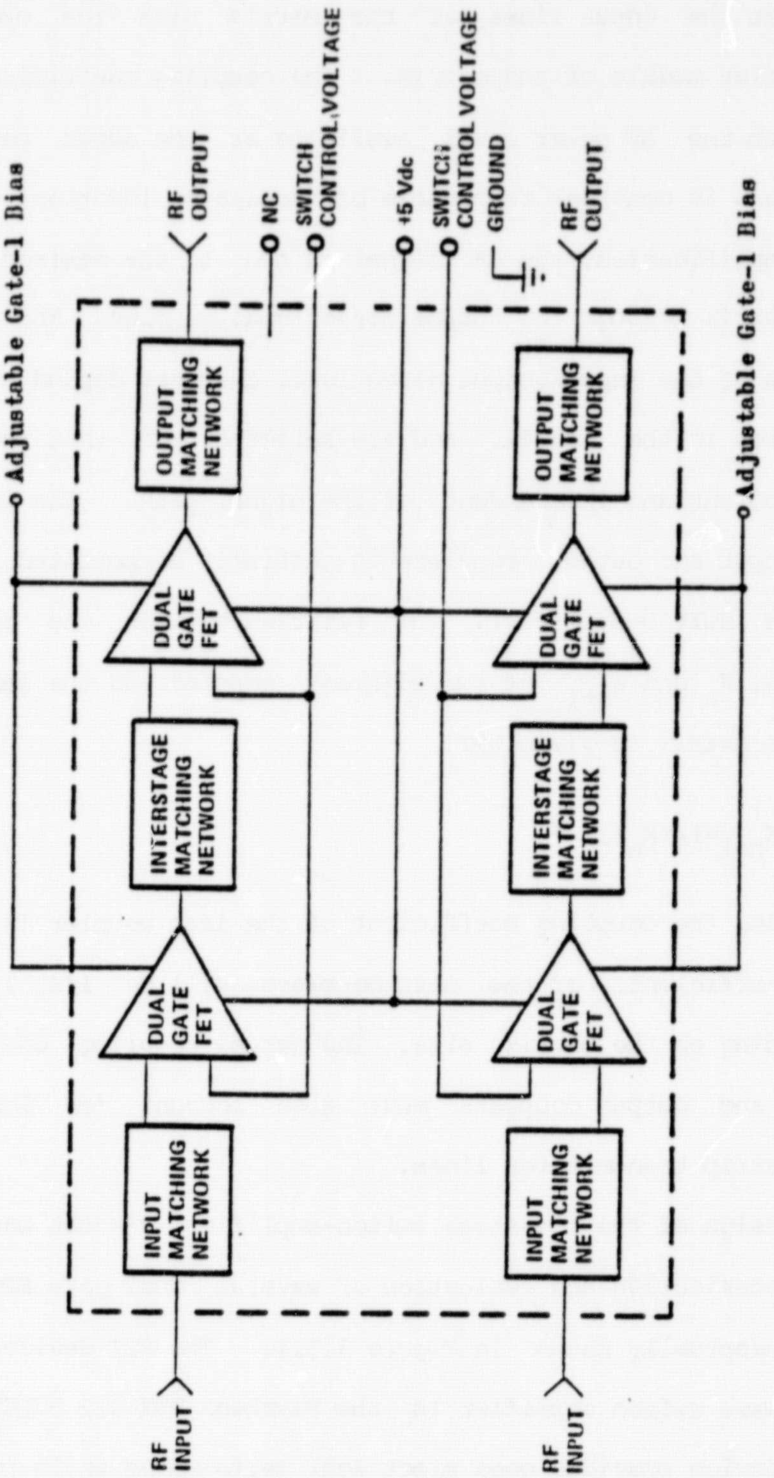
FIGURE 3.5.4

SWITCH AMPLIFIER MODULE



the FET, the interstage matching circuit was designed for a double tuned frequency response in which the gain and gain flatness are optimized for a wide frequency band between 3.5 and 6.0 GHz. A stabilizing circuit was designed for each gate-1 bias circuit to ensure unconditionally stable operation and minimize low frequency gain. The input matching circuit was designed with the additional elements to improve the "ON" and "OFF" input matching performance. The entire circuit was analyzed and optimized using the microwave analysis program SUPERCOMPACT.

The switch-driver circuit is the interface circuit between the Dual-Gate GaAs FET switch-amplifier and the distribution control unit and provides the "ON" and "OFF" control voltages to the second gate of the dual-gate FET. The switch driver module concept is shown in Figure 3.5.5. When the control voltage is zero or slightly positive, the two-stage switch amplifier is "ON". When the control voltage is sufficiently negative (e.g., -5 volts), the switch amplifier is "OFF", and the desired high isolation levels are achieved for the corresponding signal path. The capability of the switch-driver circuit to provide fast rise-time turn-on and turn-off voltages to the second gate of the Dual-Gate GaAs FET is governed by the switch-driver transistor switching speed. Low power consumption in the "ON" and "OFF" state was a requirement for the switching circuits.

Each switch driver module is associated with a pair of adjacent crosspoints of the matrix. The module contains a dual switch-driver stage using high-speed bipolar transistors controlled through a dual flip-flop integrated circuit. The actual switching is controlled by the control signal from the distribution control unit and triggered by the

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SWITCH DRIVER MODULE

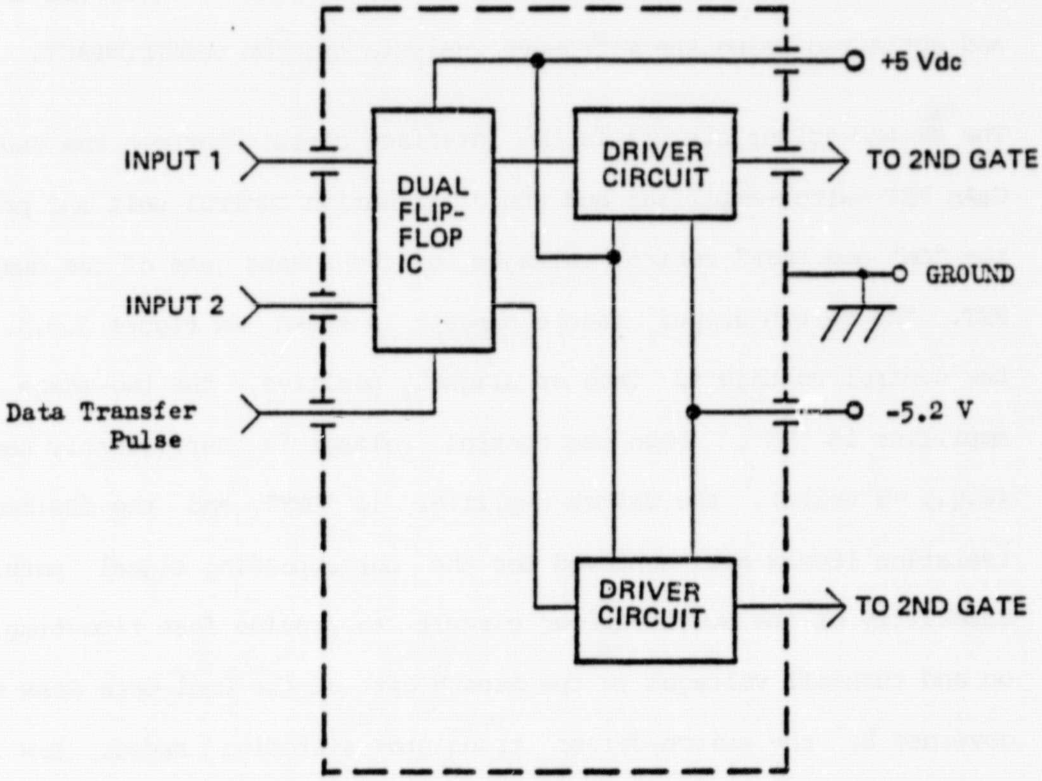

FIGURE 3.5.5

data transfer pulse, supplied also by the DCU. The data transfer pulse determines when the change of the matrix configuration is initiated.

The characteristics of the switch-driver circuit are summarized as follows:

- High-speed switching using bipolar transistors
- ON/OFF controlled by a high-speed flip-flop integrated circuit and the system data transfer pulse
- Low power consumption during the "OFF" state
- Control voltages +0.2 volts for "ON" and -5.2 volts for "OFF" states
- Modular thick-film package for two switch-drivers associated with two adjacent crosspoints

b. The Distribution Control Unit (DCU)

The DCU was designed to control a 22 x 22 microwave switch matrix consisting of 484 crosspoints. The control is exercised thru a preprogrammed memory. Sequential readout of memory contents determines a sequence of up to 256 switching configurations connecting 20 input ports to 20 output ports. Two additional inputs and outputs are provided for redundant paths in case of crosspoint switching circuit failures. The sequence of up to 256 states is repeated over a time interval called a frame.

A block diagram of the DCU is shown in Fig. 3.5.6. It consists of the following functional blocks:

1. Oscillator and Countdown Chain

DISTRIBUTION CONTROL UNIT

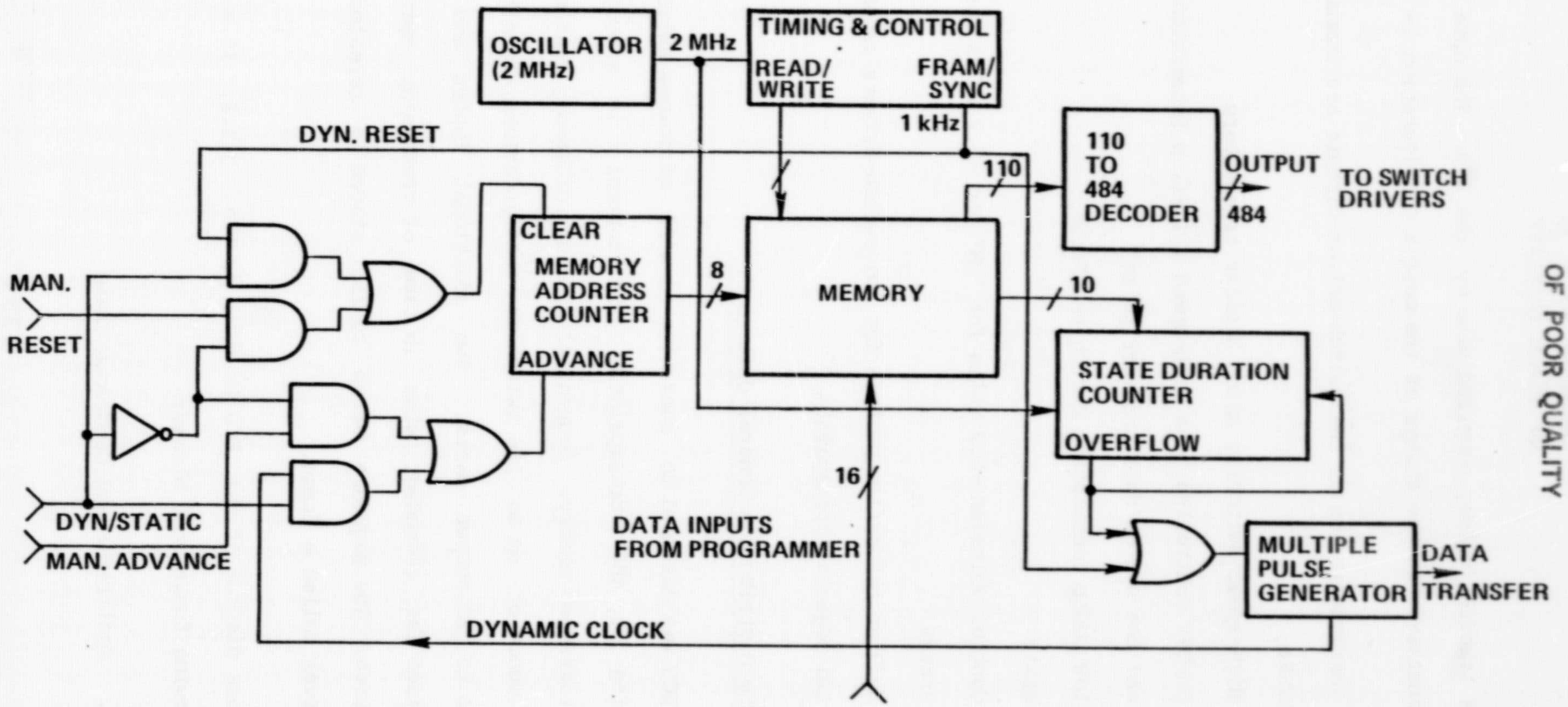

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FIGURE 3.5.6

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2. Frame Sync Generator
3. Memory
4. Memory Address Counter
5. State Duration Counter
6. Sequential Pulse Generator
7. 22 Decoders

The countdown chain starts with a 4 MHz oscillator and provides the following frequencies: 4 MHz for the sequential pulse generator, 2 MHz for the state duration counter, 1 MHz and 1 kHz for the frame sync generator and any other timing required by the circuit.

The frame sync generator provides a pulse at 1 kHz repetition rate and 1 us wide. The frame period for the DCU is 1 ms. The minimum duration of a switching configuration, otherwise called a switching state, is 1 us ($T_2 = 1/f$ where $f = 1$ MHz).

The memory required to operate the matrix is a random access memory (RAM), 124 bits wide and 256 words deep. It consists of 31 54C920 ICs in a 256 x 4 configuration . It requires eight address lines. Of the 124 bits available, 110 bits are used for matrix configuration, 11 bits are used to define the duration of each switching state and 3 bits are spares.

The memory is pre-programmed by a specially designed programming circuit as part of the special test equipment.

The memory address counter is an eight bit up-counter and supplies the eight address lines to the memory and it is cleared by the frame sync pulse. It is advanced by a pulse generated at the termination of each

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switching state and goes through all possible 256 states if the sum of all switching state durations add up to 1 ms or less. Otherwise, the frame sync will clear the counter before all states are reached.

The state duration counter is an 11 stage up-counter that determines the duration of a state. It is preloaded at the termination of each switching state by an 11 bit number from memory. When preloaded with a number N, it takes 2048-N clocks for the counter to reach overflow (all ones state). Since the clock frequency advancing this counter is 2 MHz, the duration of a state is (2048-N)/2 microseconds, where N is the preloaded state duration.

The sequential pulse generator supplies a series of pulses referenced in time to an input. Each pulse follows the other in intervals of n input clock periods of 250 ns. Each pulse is also 250 ns wide. The pulses are used to advance the memory address counter and to transfer data from memory to switch drivers.

The reference inputs to the pulse generator are the frame sync pulse or the overflow pulse from the state duration counter.

Each of the 22 decoders in the DCU controls one of the 22 columns of the matrix. Each decoder requires five bits from memory and provides 22 output bits. Only one output bit can be in the "ON" state since only one crosspoint in each column can be "ON" at any time. These output voltages are applied to the corresponding inputs of the flip-flop in the switch-driver module, i.e., one output for each crosspoint. A data transfer pulse from the sequential pulse generator transfers the data from the decoders to the storage elements of the switch drivers in the

switch matrix.

Dynamic operation starts after the desired program has been loaded into the RAM. A change in matrix configuration is initiated by the frame sync pulse. The beginning of a frame occurs at the leading edge of frame sync pulse, which sets the address counter to zero. The duration of a switching state is measured in the number of clock periods advancing the state duration counter (2 MHz). The minimum duration is two clock periods or 1 us; the maximum duration is the frame period or 1 ms.

A program stored in the memory gives an invariable sequence of configurations repeated every frame. To change the sequence, the memory has to be reprogrammed.

PACKAGING AND MECHANICAL DESIGN APPROACH

The major emphasis in the mechanical package design was to develop a unit that would minimize size, would require minimal assembly time and could easily be tuned and tested. The package consisted of two chassis mounted one on top of the other. The chassis contained two submatrices: a 22 x 12 and a 22 x 10, which formed the final 20 x 20 basic matrix plus two additional input rows and two output columns needed for redundancy (final size 22 x 22). The POC model outline dimensions are shown in Figure 3.5.1 and dimensions and weight are given in Table 3.5.1.

Each set of two crosspoints within the matrix consisted of a thin-film switch-amplifier module and a thick film switch-driver module. The input couplers and the switch-driver module were installed on one side of the chassis. The switch-amplifier modules and the output coupler substrates were installed on the opposite side. The interconnection

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TABLE 3.5.1

POC MODEL MECHANICAL CHARACTERISTICS

MECHANICAL CHARACTERISTICS

SIZE: See Outline Drawing Figure 3.5.1

IF SWITCH MATRIX:	18-3/4" x 19" x 3-1/4"
DISTRIBUTION CONTROL UNIT: (including DCU Programmer)	17" x 17" x 3-1/4"

WEIGHT

IF SWITCH MATRIX:	
Top Chassis (48 Crosspoints):	4385 grams (9 Lbs, 11 oz.)
Bottom Chassis (28 Crosspoints):	4300 grams (9 Lbs, 8 oz.)
Total Weight (including base and covers) :	19335 grams (42 Lbs, 10 oz.)
DISTRIBUTION CONTROL UNIT:	4900 grams (10 Lbs, 13 oz.)
Interconnect Cables and Connectors:	1,910 grams (4 Lbs, 3 oz.)

between the switch-amplifier/output coupler on one side and the switch-driver/input coupler on the opposite side of the chassis were made using glass-metal feedthrus. The mechanical design and layout were the key elements that minimized the parasitic elements affecting overall switching performances and controlled the size and system weight.

The distribution control unit was packaged in a separate unit and was connected to the switch matrix through a set of six 100 wire cables (terminated with multipin miniature connectors) and two coaxial cables (for data transfer pulses).

3.6 Task 6. Fabrication of POC Model and Special Equipment

In accordance with the design and specifications presented in the major design review meeting, a POC model was fabricated. Thirty-eight switch amplifier modules consisting of 76 crosspoints located as shown in Figure 3.6.1 were installed with active switching and driver circuits. All input/output couplers required for 14 input rows and 10 output columns of the matrix were installed. As equipped, the fabricated model was able to provide complete information on the performances of a 20 x 20 switch matrix. No serious problems arose during the fabrication of the POC model, but it was realized that the mechanical integration of a large matrix requires serious effort and dedication. Manufacturing and interim acceptance tests of individual modules and components were also performed during the POC model fabrication. Special tools and alignment fixtures were used in the attachment of input/output couplers to the machined aluminum chassis using silver epoxy.

The fabrication of the distribution control unit with its built-in

CROSSPOINT LOCATION DIAGRAM

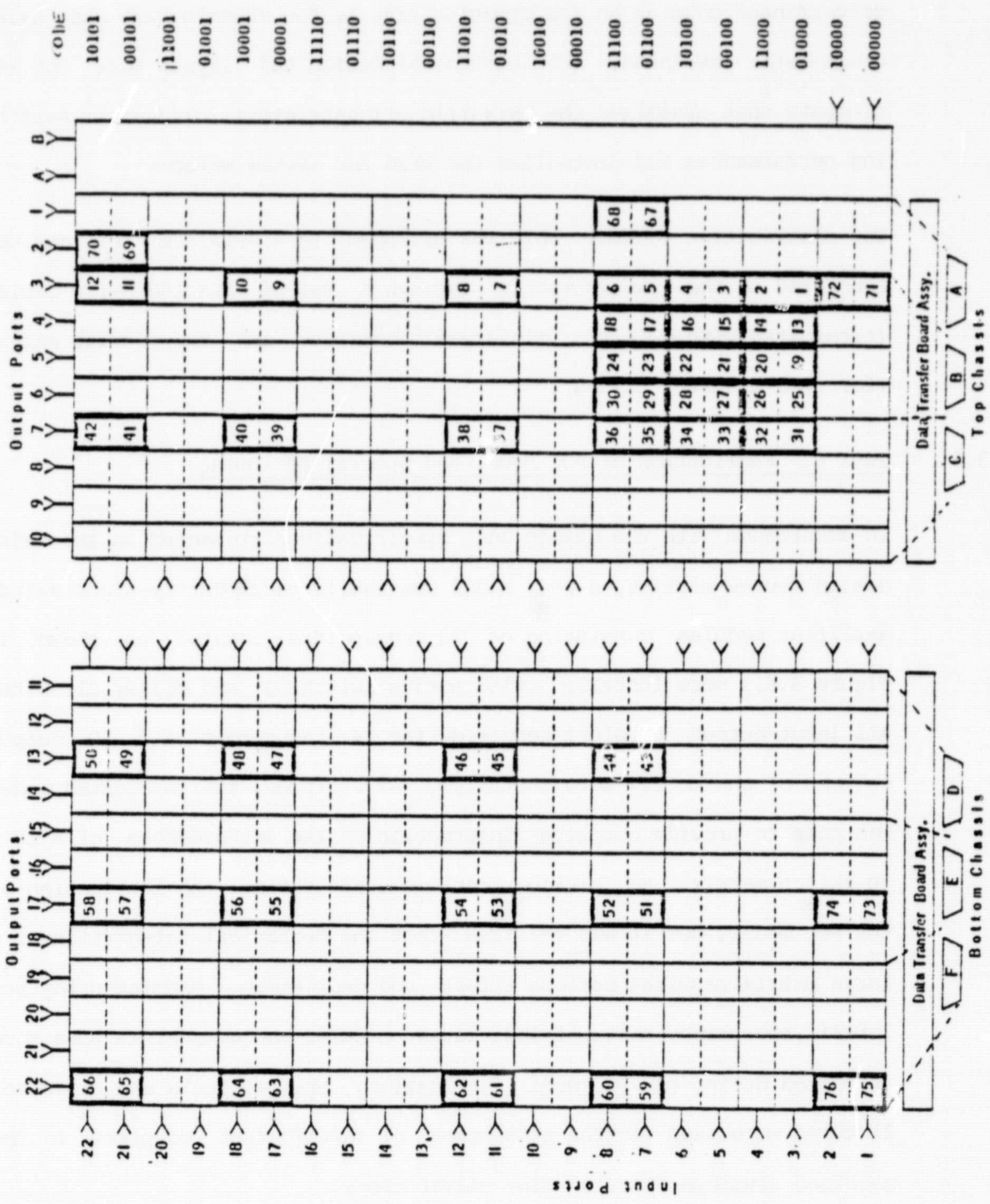

FIGURE 3.6.1 CROSSPOINT LOCATIONS

programmer was completed as designed with no major difficulties or design changes.

The final switch matrix system, consisting of the switch matrix with the interconnected distribution control unit, is presented in Fig. 3.6.2. A detail of the switch matrix with a view of the dual switch amplifier modules installed in the top tray is presented in Fig. 3.6.3. Fig. 3.6.4 shows a close-up view of the top matrix chassis.

Figs. 3.6.5 and 3.6.6 show the dual, thin film switch amplifier module and the dual, thick film switch driver module associated with each set of two crosspoints of the crossbar switch matrix. Fig. 3.6.7 shows the fully operational distribution control unit for a 20 x 20 switch matrix.

The POC switch matrix and the distribution control unit was hand carried and delivered to NASA/Lewis Research Center on December 14, 1982. At the final review held at NASA/Lewis Research Center on December 15, 1982, the fabricated and tested POC model was presented and its proper operation demonstrated.

3.7 Task 7. POC Model Testing and Analysis

The testing of the POC model which included functional and thermal-vacuum tests, were conducted at Ford Aerospace and Communications Corporation in accordance with the developed test plans and procedures. The primary operating performance tests were conducted in the presence of Mr. E. W. Spisz, NASA Program Manager, starting November 1, 1983. All test data, results, and Data Analysis have been compiled in a comprehensive Task VII report including test details, plots, test set-ups, and performance statistical analysis.

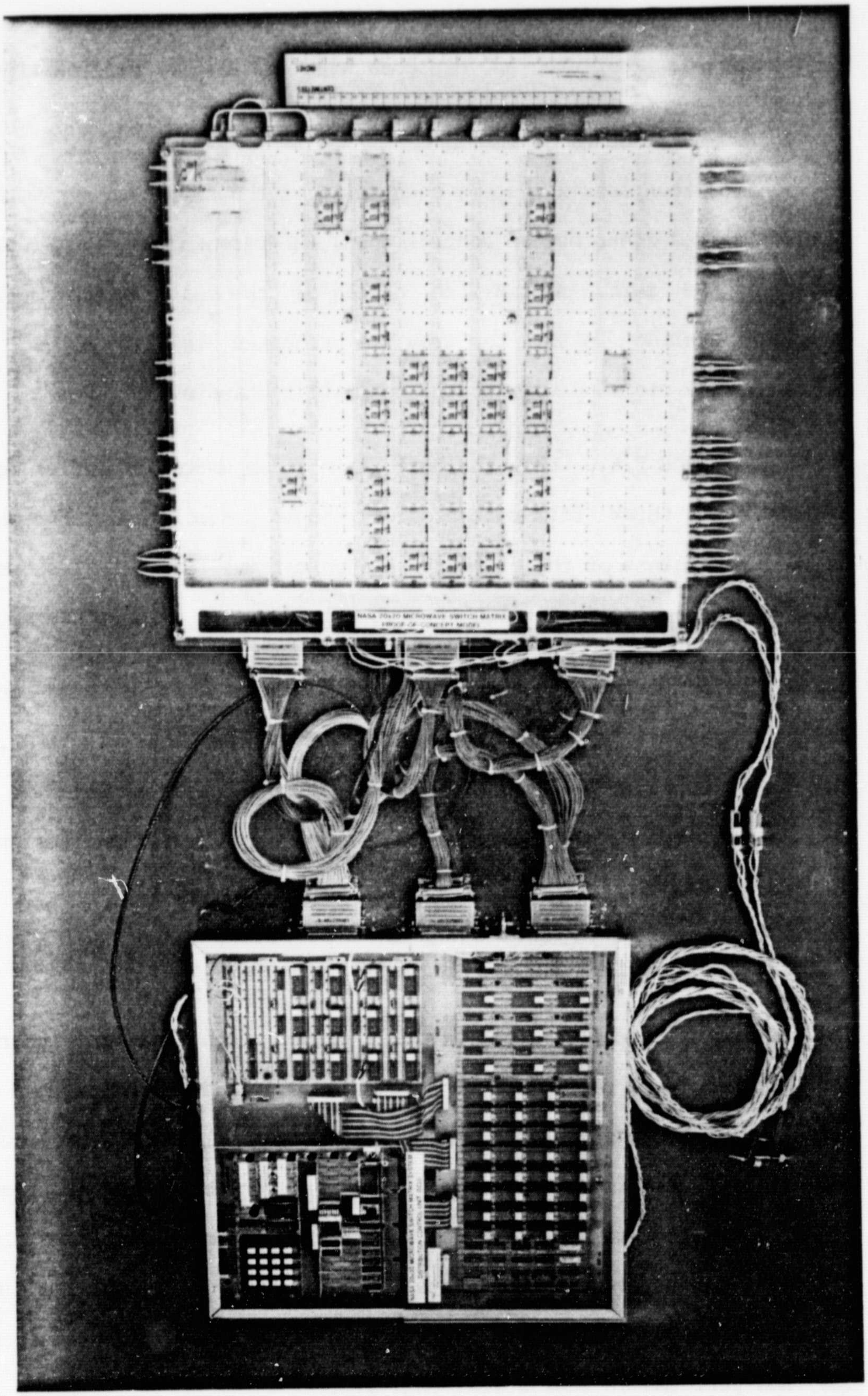

FIGURE 3.6.2 20 x 20 MICROWAVE SWITCH MATRIX SYSTEM
(PROOF-OF-CONCEPT MODEL)

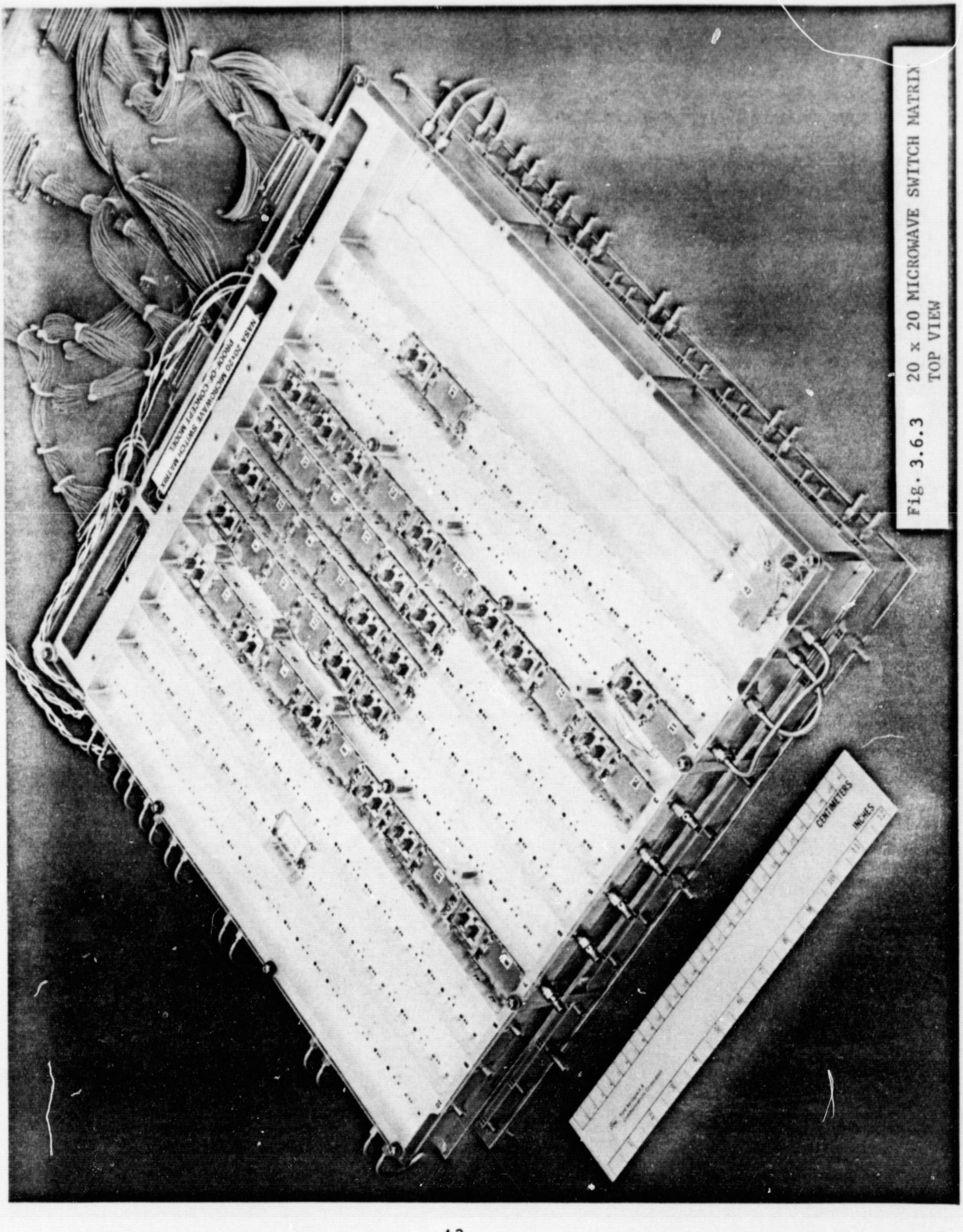

Fig. 3.6.3 20 x 20 MICROWAVE SWITCH MATRIX
TOP VIEW

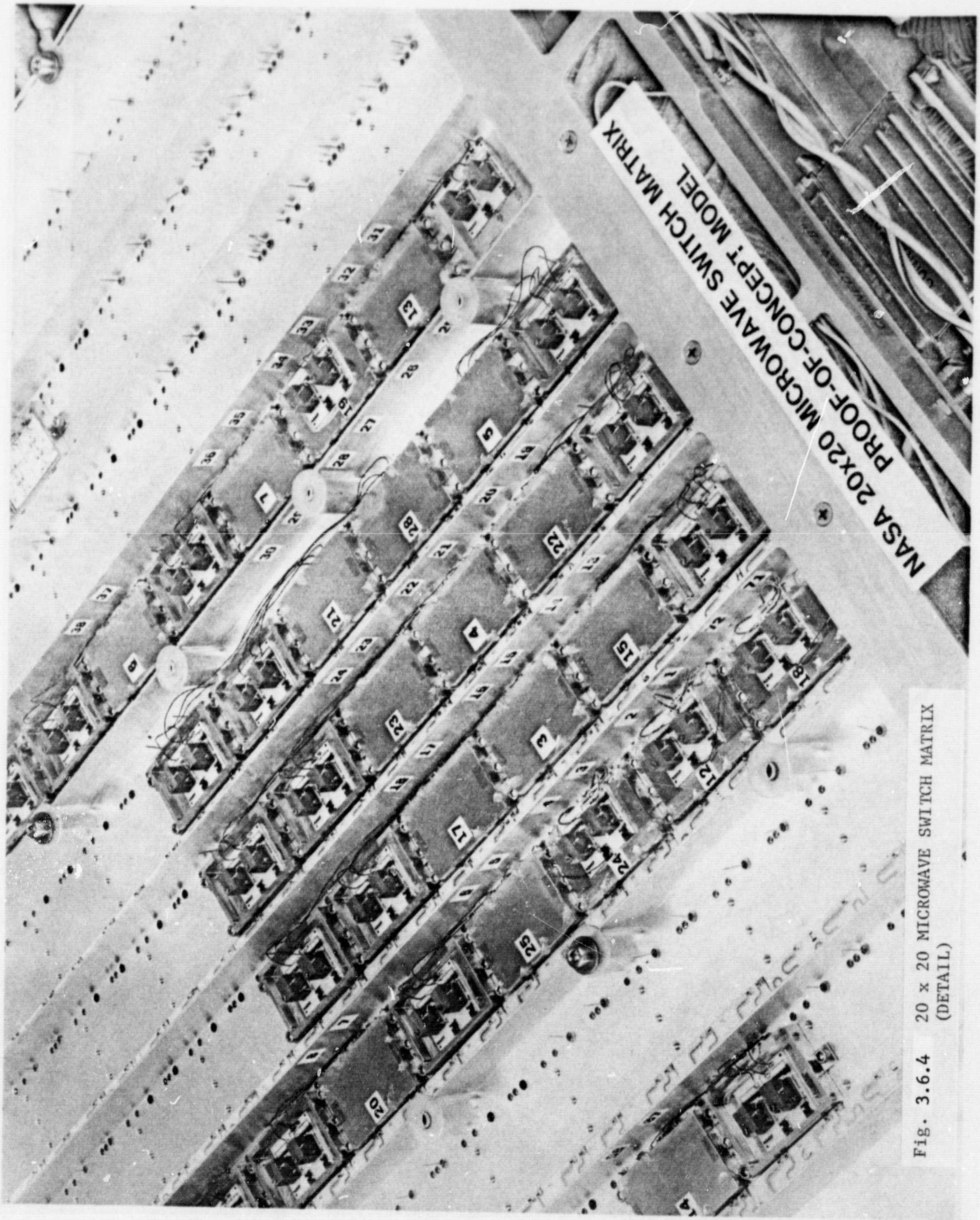

Fig. 3.6.4 20 x 20 MICROWAVE SWITCH MATRIX (DETAIL)

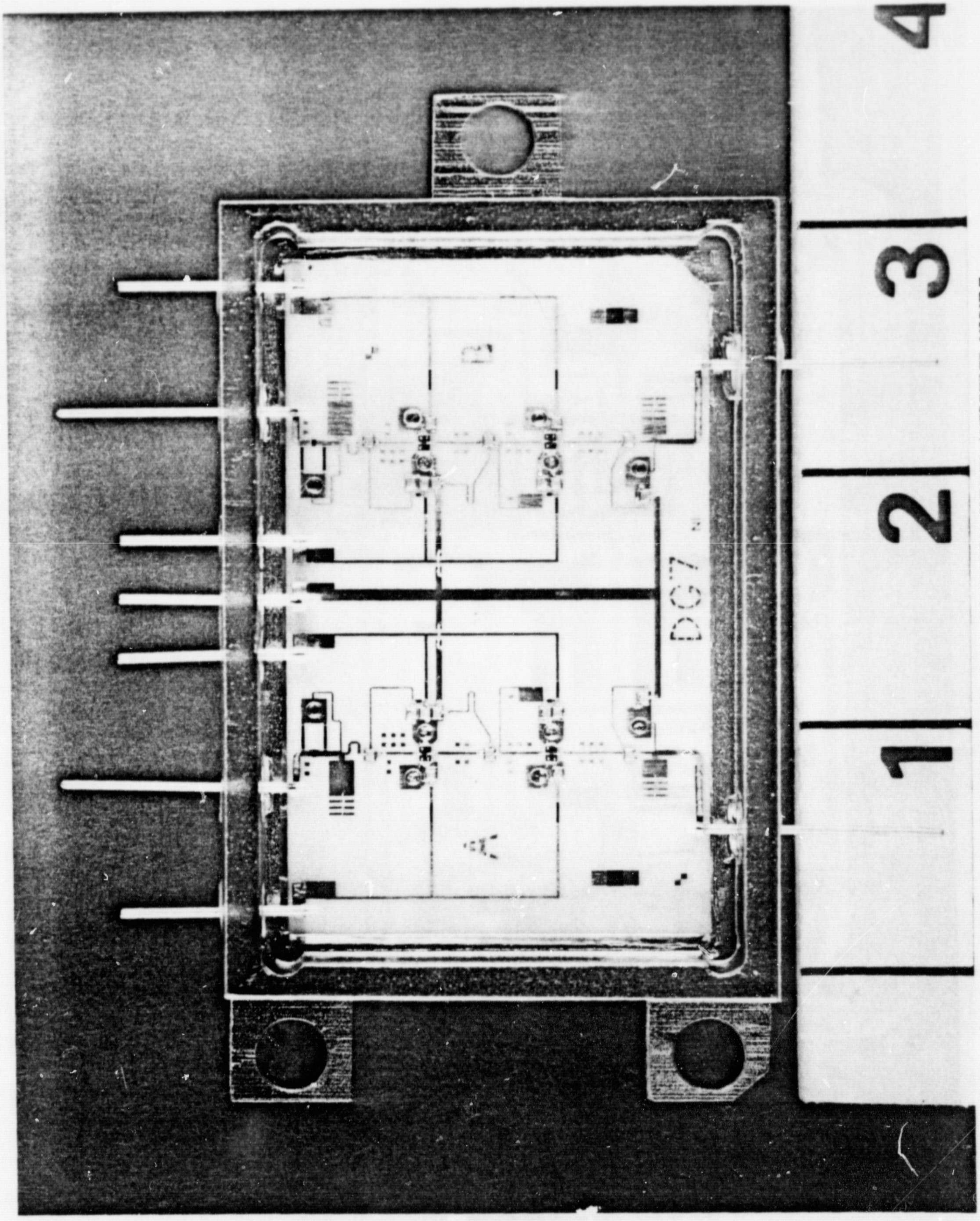

FIGURE 3.6.5 DUAL THIN-FILM SWITCH-AMPLIFIER MODULE

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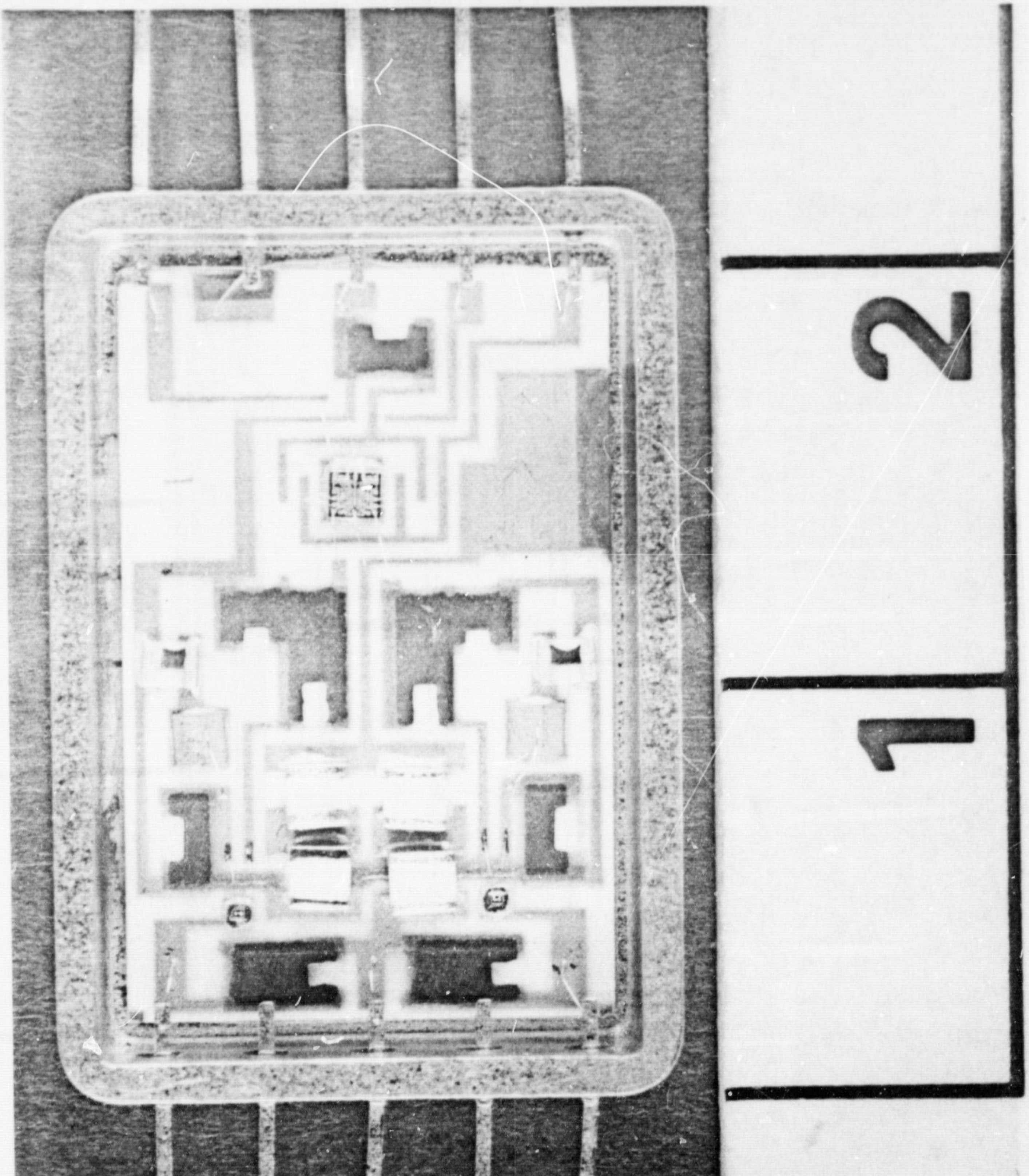

FIGURE 3.6.6 DUAL THICK-FILM SWITCH-DRIVER MODULE

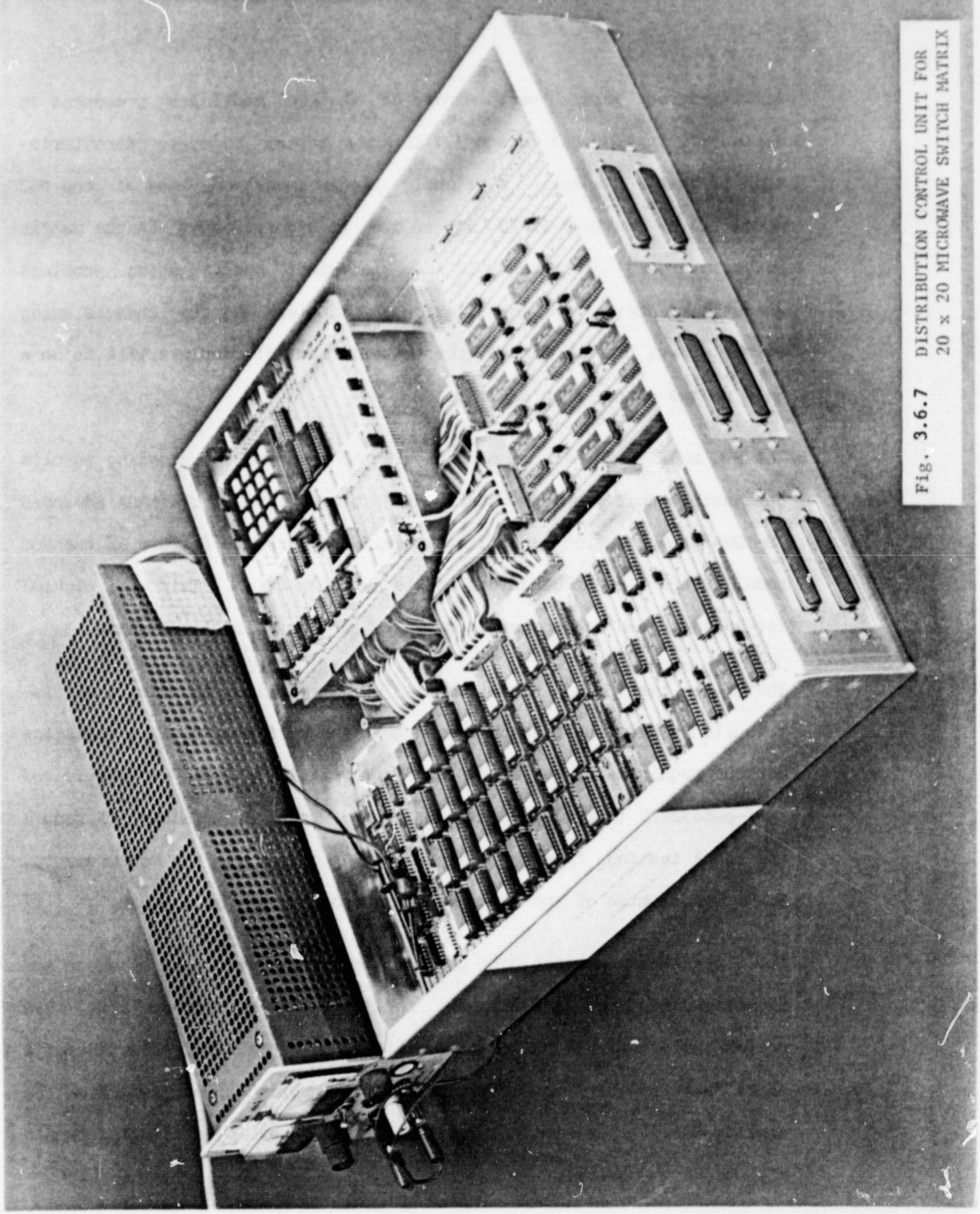

Fig. 3.6.7 DISTRIBUTION CONTROL UNIT FOR
20 x 20 MICROWAVE SWITCH MATRIX

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Specifications versus performances of the POC model are presented in Table 3.7.1. Fig. 3.7.1a and 3.7.1b show typical bandpass characteristics of the POC model. A slightly higher insertion loss of the POC model (20 dB instead of 18 dB) is due to higher losses in the matrix couplers. This discrepancy is due to minor manufacturing problems encountered during the installation of couplers to the chassis using silver epoxy. In the future, the installation of couplers will be on a gold plated rather than aluminum chassis.

The POC model has been thoroughly tested and the outstanding results demonstrate that a switch matrix could be developed for a NASA advanced SS-TDMA communication satellite system. A remarkable feature of the POC model is the 2.5 GHz bandwidth of the switch matrix . This will provide for an increased communication capacity for communication systems.

The final testing of the microwave switch matrix, incuding the distribution control unit demonstrated that the performance characteristics met the requirements for a SD-TDMA communication system. Automatic and semi-automatic test setups have been used wherever possible to reduce the final testing time and increase the accuracy of the measurements. Power consumption of the POC model is summarized in Table 3.7.2.

The distribution control unit provided the system with very accurate and flexible switching capabilities. During the 1 msec frame time, 256 states (switch matrix configurations) are possible. The selection of a state duration of 1 ms or longer will establish a non-switching or static mode of operation. State durations 1 us or longer (in increments of 1 us) are possible.

SPECIFICATION VS PERFORMANCE

PARAMETER		SPECIFICATION	PERFORMANCE
MATRIX SIZE		20 x 20	20 x 20
CONNECTIVITY		76 ACTIVE X-POINTS	76 12 ACTIVE INPUTS 8 ACTIVE OUTPUTS
FRAME DURATION		1 ms	1 ms
NUMBER OF STATES PER FRAME		N/A	256
RECONFIGURATION RATE		2 μs	1 μs
SWITCHING SPEED		10 ηs	5 ηs
IF FREQUENCY		3.5 TO 6.00 GHz	3.5 TO 6.0 GHz
IF BANDWIDTH		2.5 GHz	2.5 GHz
INSERTION LOSS		18 dB	20 dB
GAIN/INSERTION LOSS RIPPLE		1.0 dB PER 1 GHz	< 1 dB PER 1 GHz
PHASE LINEARITY		± 5 DEGREES	± 5 DEGREES
ISOLATION		40 dB	> 45 dB
INPUT VSWR		1.5:1	< 1.5:1
OUTPUT VSWR		1.5:1	1.5:1
INPUT SIGNAL LEVEL		-30 dBm → -10 dBm	-15 dBm → +10 dBm
1 dB COMPRESSION POINT		N/A	+16 dBm
MAX INPUT SIGNAL		+10.0 dBm	> +16 dBm
NOISE LEVEL (BELOW OUTPUT LEVEL)		35 dB	> 50 dB AT -5 dBm INPUT
	MATRIX	N/A	18.75" x 19" x 3.25"
	DCU	N/A	17" x 17" x 3.25"
CONSUMPTION (76 CROSSPOINTS)			
	MATRIX	N/A	5.7 WATTS
	DCU	N/A	6.25 WATTS
WEIGHT (76 CROSSPOINTS)			
	MATRIX	N/A	8.685 kg (19 lb, 3 oz)
	DCU	N/A	4.900 kg (10 lb, 13 oz)

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Table 3.7.1

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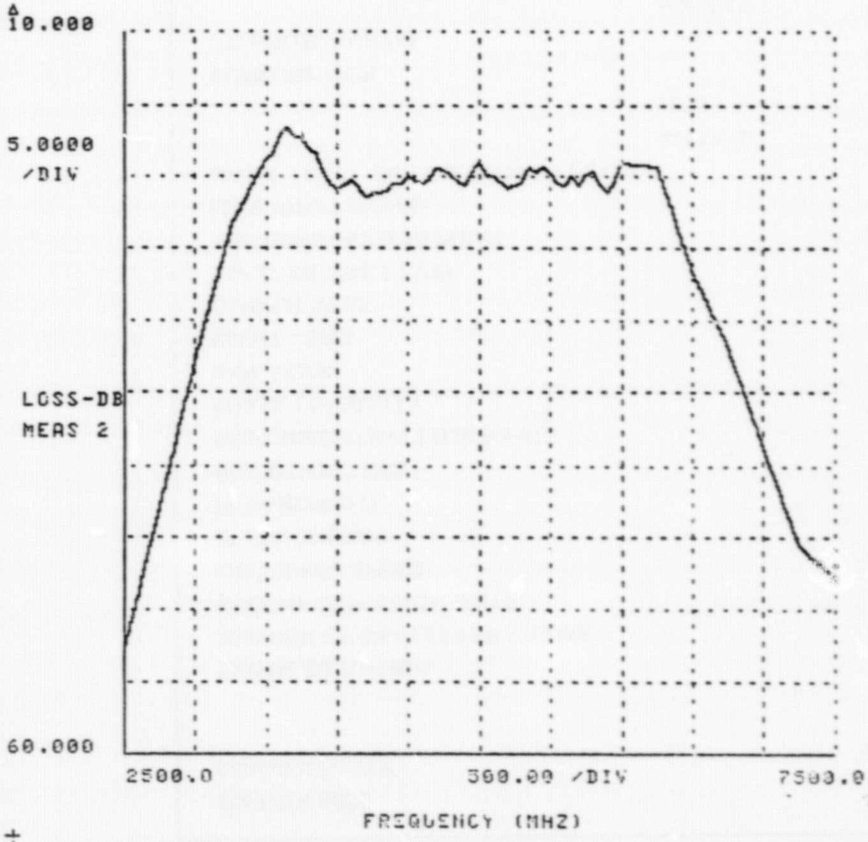
FIGURE 3.7.1a

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#45 IN-11 OUT-13



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#45 IN-11 OUT-13

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	82.81	1.13	24.44	52.84	-7.43	.91
2750.000	69.44	1.02	40.13	42.98	-83.07	.91
3000.000	81.39	1.35	16.50	33.08	-171.91	1.20
3250.000	88.82	1.16	22.41	23.52	60.59	1.50
3500.000	75.19	1.27	18.50	18.80	-81.67	2.20
3550.000	74.63	1.29	18.05	18.49	-177.50	5.38
3600.000	73.22	1.15	23.29	17.03	84.65	5.7[illegible]
3650.000	86.10	1.58	13.00	16.61	-24.10	5.82
3700.000	74.72	1.60	12.68	17.25	-124.96	5.54
3750.000	91.46	1.22	20.20	17.32	136.55	5.48
3800.000	82.22	1.15	23.30	18.06	37.72	5.51
3850.000	84.60	1.21	20.54	18.37	-61.77	5.44
3900.000	76.89	1.26	18.81	19.71	-158.28	5.19
3950.000	78.92	1.09	27.42	20.57	111.58	4.99
4000.000	73.57	1.11	25.63	20.85	21.95	5.03
4050.000	65.72	1.09	27.04	20.62	-69.37	5.15
4100.000	76.21	1.24	19.55	20.32	-163.62	5.27
4150.000	72.03	1.06	30.19	20.84	100.77	5.14
4200.000	72.92	1.36	16.02	21.46	11.45	5.01
4250.000	74.57	1.27	18.51	21.21	-79.66	5.06
4300.000	73.06	1.16	22.49	21.14	-170.62	5.03
4350.000	78.45	1.07	29.75	20.97	95.37	5.14
4400.000	62.07	1.40	15.51	20.51	4.47	5.21
4450.000	66.62	1.52	13.75	20.56	-88.19	5.16
4500.000	66.29	1.24	19.25	19.97	178.71	5.26
4550.000	68.89	1.21	20.27	20.33	82.59	5.15
4600.000	69.96	1.50	13.96	20.55	-6.83	5.10
4650.000	75.42	1.42	15.20	20.23	-101.01	5.16
4700.000	68.49	1.40	15.55	19.44	167.43	5.32
4750.000	73.31	1.27	16.48	19.57	67.55	5.37
4800.000	76.24	1.25	19.09	19.93	-25.93	5.15
4850.000	68.39	1.13	24.30	20.37	-117.99	5.15
4900.000	64.81	1.57	13.10	20.60	148.77	4.96
4950.000	67.29	1.74	11.35	19.65	63.59	5.19
5000.000	72.08	1.40	15.65	18.96	-37.91	5.50
5050.000	69.19	1.53	13.63	19.89	-134.40	5.27
5100.000	68.65	1.47	14.47	19.95	132.32	5.18
5150.000	69.86	1.59	12.64	20.40	39.05	5.13
5200.000	70.45	1.48	14.31	20.67	-32.47	5.03
5250.000	67.84	1.46	14.56	20.59	-142.07	5.01
5300.000	68.71	1.54	13.46	20.42	127.26	5.18
5350.000	82.26	1.42	15.20	19.37	31.34	5.38
5400.000	75.51	1.50	13.99	19.72	-66.53	5.32
5450.000	72.48	1.55	13.27	19.40	-160.31	5.38
5500.000	81.49	1.31	17.40	19.76	99.79	5.34
5550.000	81.50	1.41	15.42	20.50	7.38	5.39
5600.000	72.73	1.05	31.81	20.66	-33.23	5.14
5650.000	69.03	1.24	19.47	19.09	-177.34	5.27
5700.000	76.65	1.33	17.09	23.34	37.08	3.17
5750.000	69.60	1.54	13.31	19.92	-3.57	3.33
5800.000	73.40	1.82	10.74	19.63	-104.77	3.50
5850.000	70.24	2.17	3.67	20.61	132.33	3.17
5900.000	72.63	1.96	9.80	21.15	69.08	4.92
5950.000	81.47	2.15	8.77	20.41	-18.87	5.19
6000.000	70.60	1.83	10.64	19.11	-117.54	2.44
6250.000	71.04	1.51	13.08	19.29	73.29	1.33
6500.000	90.07	2.12	3.39	26.60	-32.73	1.41
6750.000	80.60	1.13	24.05	31.73	-174.33	1.25
7000.000	69.67	1.41	15.38	39.34	99.80	1.05
7250.000	76.92	1.32	10.72	43.57	-6.49	1.13
7500.000	77.49	1.53	13.52	47.76	-104.25	1.13

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

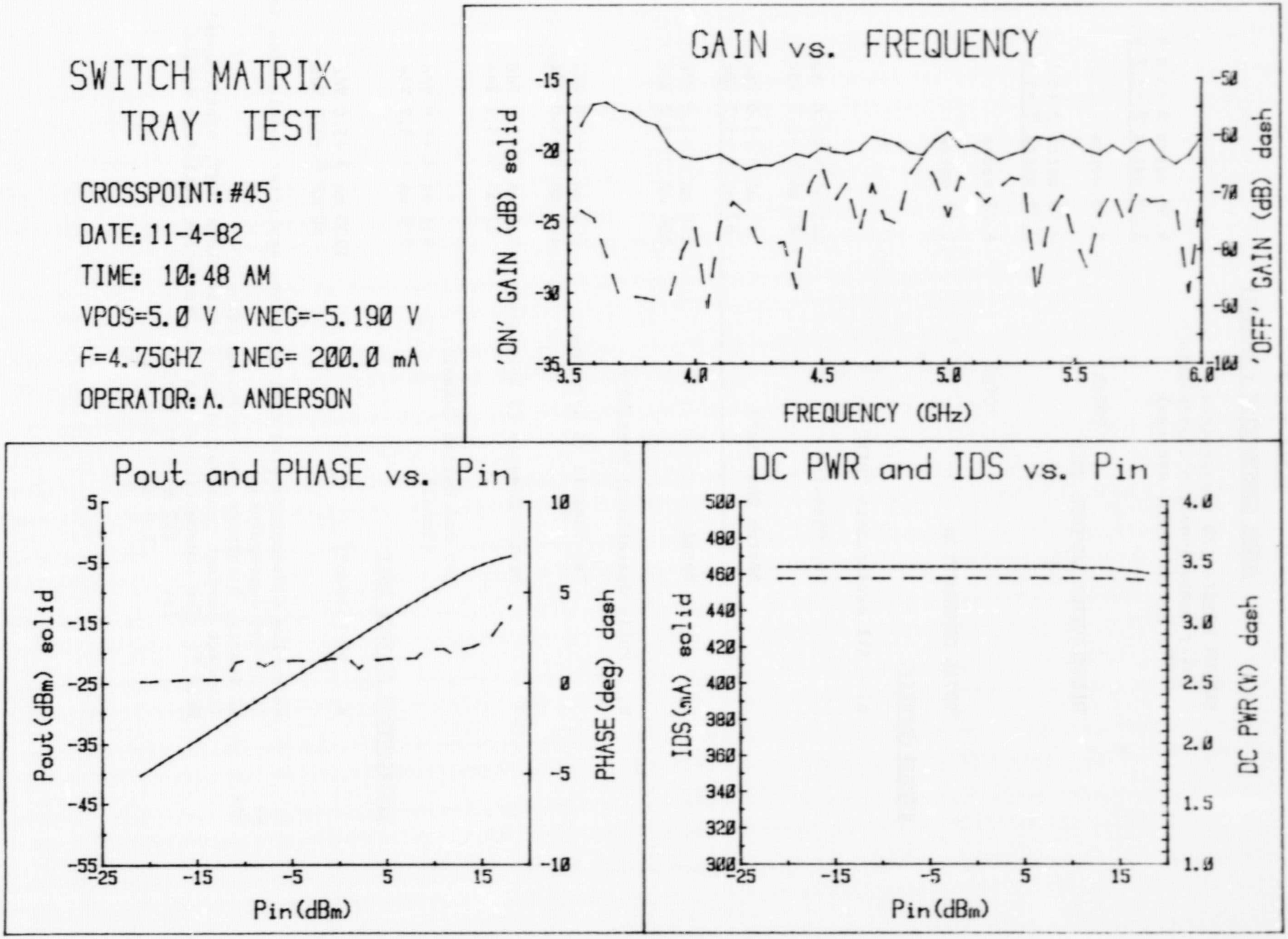

SWITCH MATRIX
TRAY TEST
CROSSPOINT: #45
DATE: 11-4-82
TIME: 10:48 AM
VPOS=5.0 V VNEG=-5.190 V
F=4.75GHZ INEG= 200.0 mA
OPERATOR: A. ANDERSON
GAIN vs. FREQUENCY
'ON' GAIN (dB) solid
'OFF' GAIN (dB) dash
FREQUENCY (GHz)
-15
-20
-25
-30
-35
-50
-60
-70
-80
-90
-100
3.5
4.0
4.5
5.0
5.5
6.0
Pout and PHASE vs. Pin
Pout (dBm) solid
PHASE (deg) dash
Pin (dBm)
5
-5
-15
-25
-35
-45
-55
10
0
-10
DC PWR and IDS vs. Pin
IDS (mA) solid
DC PWR (W) dash
Pin (dBm)
500
480
460
440
420
400
380
360
340
320
300
4.0
3.5
3.0
2.5
2.0
1.5
1.0
-25
-15
-5
15

FIGURE 3.7.1b

TABLE 3.7.2

POWER CONSUMPTION (SUMMARY)

SWITCH MATRIX (78 crosspoints, fully operational, 8 crosspoints "ON", static mode, average)		4.58 watts @ +5.0 V
		1.09 watts @ -5.2 V
	TOTAL	5.67 watts
DISTRIBUTION CONTROL UNIT		
		6.00 watts @ +5 V
		0.26 watts @ -5 V
	TOTAL	6.26 watts
TOTAL CONSUMPTION		11.77 watts

SWITCH MATRIX:

a. All crosspoints "OFF"

Top Chassis*	285 mA @ +5.0 Vdc
	87 mA @ -5.2 Vdc
Bottom Chassis**	91 mA @ +5.0 Vdc
	67 mA @ -5.2 Vdc
Total	375 mA @ +5.0 Vdc
	154 mA @ -5.2 Vdc

b. Fully Operational Matrix***

Top Chassis (5 X-Points):	600 mA @ +5.0 Vdc
	123 mA @ -5.0 Vdc
Bottom Chassis (3 X-Points):	315 mA @ +5.0 Vdc
	87 mA @ -5.2 Vdc
Top and Bottom Chassis: (Total)	915 mA @ +5.0 Vdc
	210 mA @ -5.2 Vdc

DISTRIBUTION CONTROL UNIT

a. DC Current:	1200 mA @ +5.0 Vdc
	50 mA @ -5.2 Vdc

* 48 active crosspoints plus dual redundant amplifier module (see Note 1)
** 28 active crosspoints
*** 12 inputs, 8 outputs, no redundant paths
(average current consumption for 8 crosspoints "ON", static mode)

Note 1: The consumption of the dual redundant amplifier module is: 120 mA @ +5.0 Vdc
1.8 mA @ -5.2 Vdc

Fig. 3.7.2(a) presents a typical RF output signal for state duration of 1 us. Figs. 3.7.2(b) and 3.7.2(c) show details of the switching state and demonstrate turn-on and turn-off switching speeds which are less than 5 ns.

The transition from one state configuration to another could be performed in approximately 10 ns and it is affected by an additional delay introduced by the signal propagation time along the microstrip transmission lines of the matrix.

This additional delay depends on the location of the crosspoint within the matrix layout and could be compensated for by delaying the data transfer pulse which triggers the switches associated with each crosspoint. Fig. 3.7.3 presents the switching time for two adjacent crosspoints on the same output port of the matrix. This figure presents the signal at the output port #22 when the signal from the input port #21 is switched off by crosspoint #65 and simultaneously the input signal from port #22 is turned on by crosspoint #66.

Fig. 3.7.4 shows the output signal for switching states of 4 us and 10 us. Fig. 3.7.5 shows the output signal for longer state durations in the broadcast mode of operation. Other switching features of the matrix have been tested for different state durations. They include the broadcast mode of operation and the redundant mode of operation.

A statistical summary of insertion loss, isolation and input VSWR for the 66 active crosspoints of the matrix is presented in Tables 3.7.3.

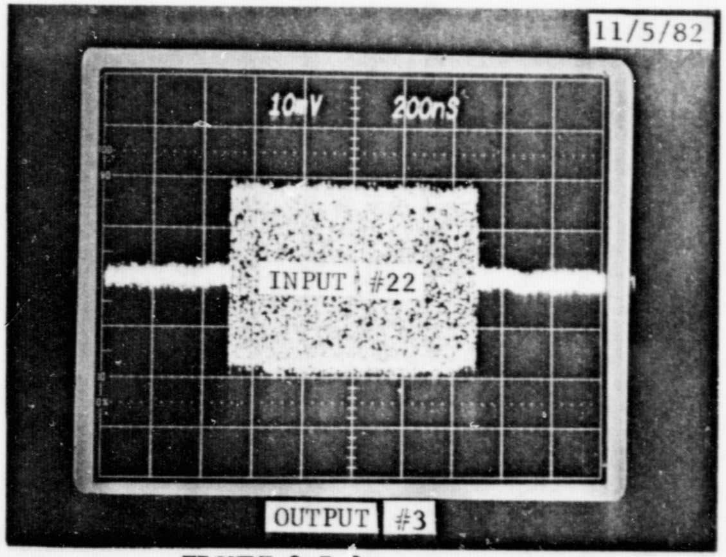


FIGURE 3.7.2a

(a)
STATE DURATION
1 μs "ON"
4 μs "OFF"

(b)
DETAIL
TURN-ON
TIME

(c)
DETAIL
TURN-OFF
TIME

TYPICAL OUTPUT SIGNAL
SHOWING SWITCHING DURATIONS
OF LESS THAN 5 ns

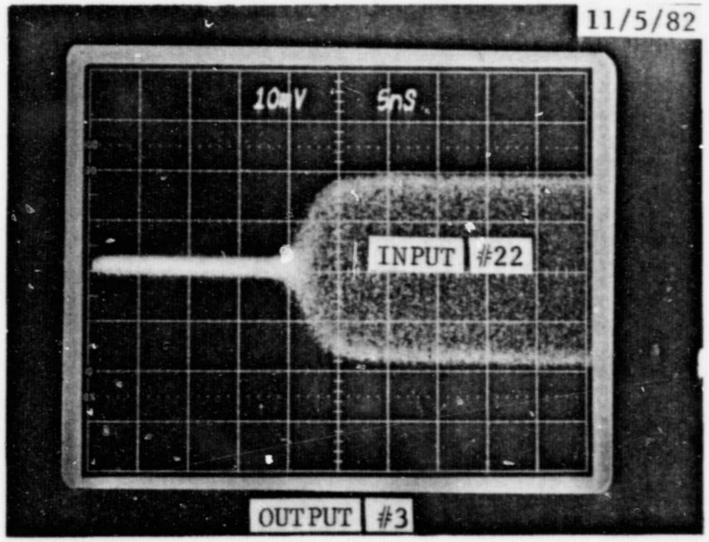


FIGURE 3.7.2b

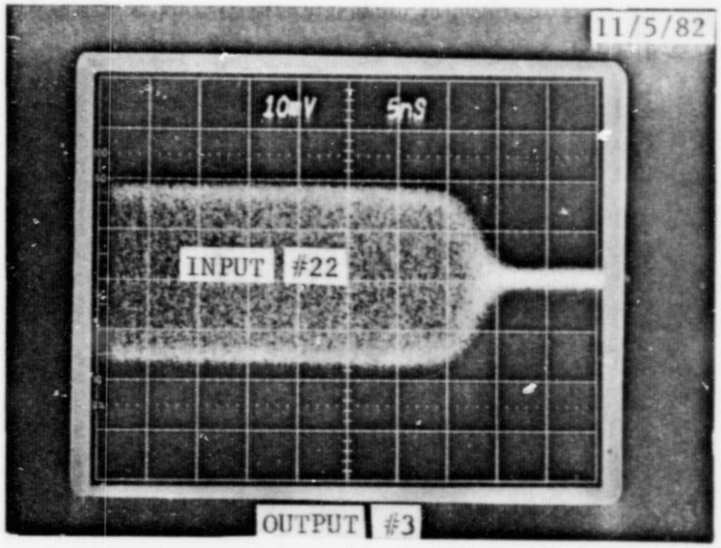
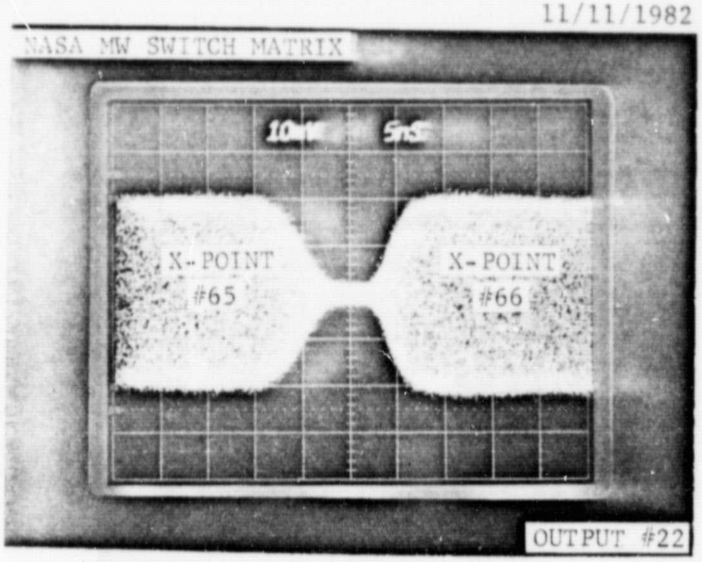
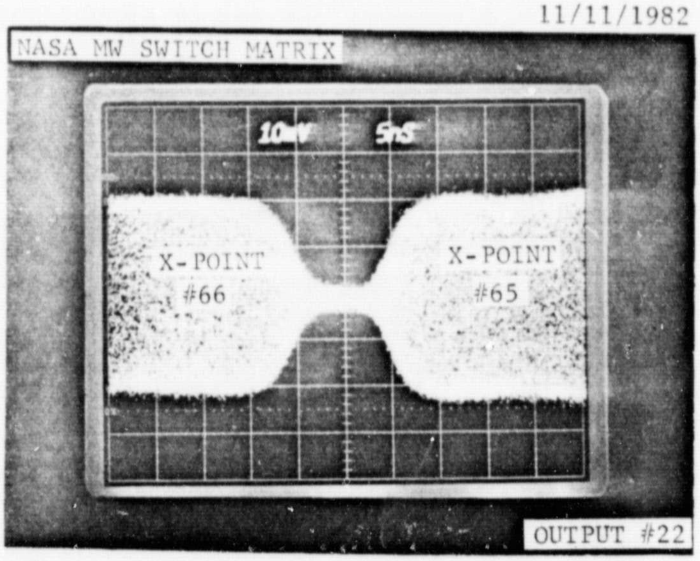


FIGURE 3.7.2c



X-POINT #65   SWITCHED "OFF"
X-POINT #66   SWITCHED "ON"



X-POINT #66 SWITCHED "OFF"
X-POINT #65 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

FIG. 3.7.3

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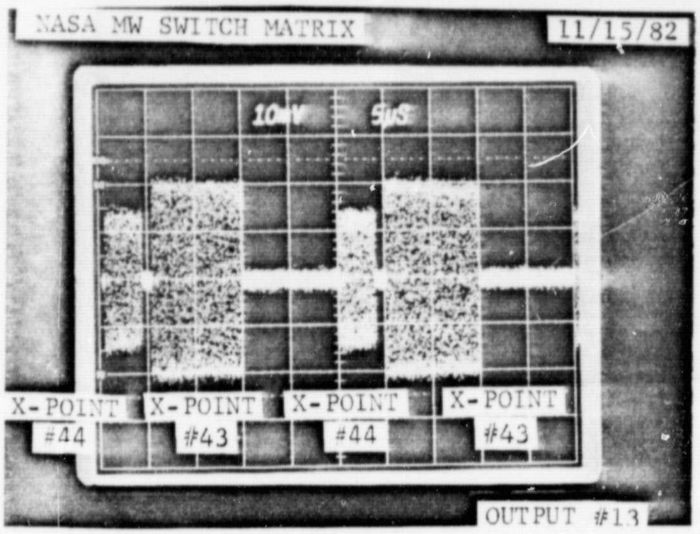

STATE DURATIONS
ON: 4 µs
OFF: 1 µs
ON: 10 µs
OFF: 10 µs

Fig. 3.7.4 OUTPUT SIGNAL AT PORT #13 FOR SWITCH DURATIONS OF 4 MICROSECONDS AND 10 MICROSECONDS. INPUT PORT #7 (Crosspoint #43) and INPUT PORT #8 (Crosspoint #44)

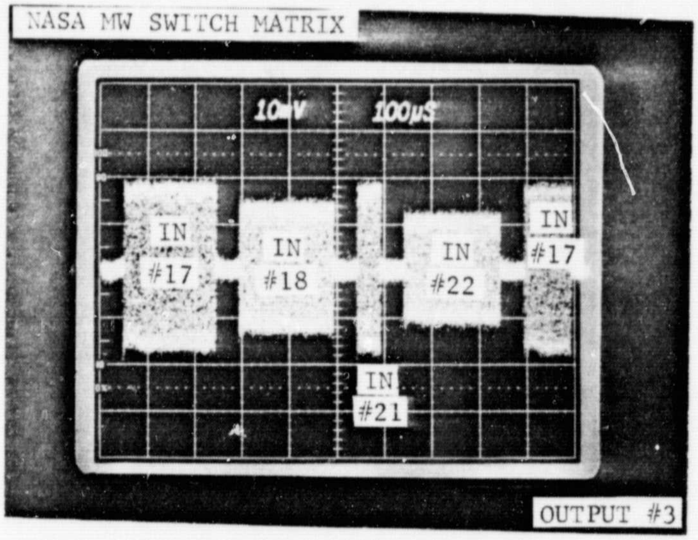

Fig. 3.7.5 OUTPUT SIGNAL AT PORT #17 FOR SWITCH DURATIONS OF 50 MICROSECONDS AND 100 MICROSECONDS. (BROADCAST MODE INPUT PORTS NUMBERS 17, 18, 21, 22)

TABLE 3.7.3

AUTOMATIC NETWORK ANALYSER TEST SUMMARY

(4 GHz to 6 GHz)

X-Point #	Isolation (dB)			VSWR			Insertion Loss (dB)		
	$\bar{X}$	S	S^2	X	$\bar{S}$	S^2	X	S	S^2
1	77.15	8.28	68.62	1.43	0.26	0.07	20.25	1.62	2.63
2	81.30	5.45	29.75	1.43	0.23	0.05	21.98	1.06	1.12
3	76.94	5.94	35.33	1.37	0.23	0.05	21.42	0.98	0.96
4	77.72	7.75	60.01	1.61	0.41	0.17	21.23	1.18	1.39
5	77.37	5.81	33.74	1.27	0.19	0.04	21.95	0.95	0.91
6	76.39	4.52	20.43	1.52	0.41	0.17	20.54	2.20	4.85
7	74.23	5.51	30.41	1.43	0.27	0.07	21.42	0.75	0.56
8	76.63	5.35	28.67	1.85	0.70	0.49	21.14	0.89	0.79
9	74.01	6.04	36.50	1.51	0.35	0.12	19.22	0.88	0.77
10	74.54	5.37	28.79	1.46	0.33	0.11	22.90	0.74	0.55
11	71.63	4.69	22.01	1.44	0.26	0.07	19.53	0.82	0.68
12	73.24	5.07	25.66	1.59	0.40	0.16	20.05	0.98	0.97
13	76.32	5.41	29.25	1.43	0.27	0.07	22.47	0.85	0.73
14	78.37	6.67	44.44	1.42	0.23	0.05	22.57	1.05	1.10
15	77.39	6.57	43.16	1.37	0.23	0.05	22.43	1.16	1.35
16	76.42	6.69	44.80	1.61	0.41	0.17	22.79	0.74	0.54
17	76.66	6.96	48.40	1.27	0.19	0.04	19.46	0.93	0.87
18	77.96	6.19	38.29	1.53	0.42	0.17	22.11	0.78	0.62
19	75.24	6.37	40.61	1.43	0.27	0.07	20.07	0.84	0.71
20	75.86	5.22	27.30	1.43	0.23	0.05	20.88	1.10	1.22

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X-Point #	Isolation $\bar{X}$	Isolation S	Isolation S^2	VSWR $\bar{X}$	VSWR S	VSWR S^2	Loss $\bar{X}$	Loss S	Loss S^2
21	74.24	5.45	29.69	1.37	0.23	0.05	21.65	0.85	0.72
22	72.18	7.03	49.37	1.61	0.41	0.17	23.02	0.94	0.89
23	69.03	4.88	23.79	1.27	0.19	0.04	19.63	1.91	3.66
24	71.83	3.87	15.01	1.52	0.42	0.17	23.52	1.08	1.17
25	76.34	8.14	66.19	1.43	0.26	0.07	20.01	0.90	0.81
26	77.23	6.04	36.44	1.43	0.23	0.05	20.12	3.31	10.94
27	77.66	7.46	55.69	1.37	0.23	0.05	19.97	1.19	1.41
28	75.86	5.31	28.18	1.61	0.41	0.17	21.59	1.47	2.16
29	76.78	5.62	31.54	1.27	0.19	0.04	22.14	0.83	0.69
30	78.29	5.03	25.29	1.53	0.42	0.17	19.21	1.11	1.24
31	75.80	6.38	40.74	1.43	0.27	0.07	21.21	1.34	1.81
32	77.74	6.18	38.21	1.42	0.22	0.05	22.39	1.22	1.50
33	75.71	6.07	36.81	1.36	0.22	0.05	20.86	1.34	1.79
34	76.62	5.36	28.72	1.61	0.41	0.17	19.43	1.89	3.56
35	78.42	7.46	55.69	1.27	0.19	0.04	19.90	1.51	2.29
36	77.75	5.78	33.42	1.53	0.42	0.17	20.24	1.42	2.02
37	74.02	5.37	28.86	1.43	0.27	0.08	21.84	1.39	1.92
38	75.20	6.17	38.13	1.84	0.68	0.47	20.09	1.28	1.65
39	71.52	5.11	26.13	1.51	0.36	0.13	19.07	0.92	0.85
40	71.70	4.66	21.74	1.46	0.33	0.11	18.91	0.77	0.60

X-Point #	Isolation $\bar{X}$	Isolation S	Isolation S^2	VSWR $\bar{X}$	VSWR S	VSWR S^2	Loss $\bar{X}$	Loss S	Loss S^2
41	69.26	3.57	12.78	1.44	0.27	0.07	18.07	0.79	0.62
42									
43	72.99	5.73	32.81	1.26	0.19	0.04	19.36	0.91	0.84
44	71.50	5.65	31.87	1.52	0.41	0.17	19.75	0.99	0.98
45	72.94	5.04	25.39	1.43	0.27	0.08	20.27	0.59	0.35
46	71.79	3.98	15.85	1.84	0.69	0.48	18.28	1.00	1.00
47	71.46	8.34	69.49	1.51	0.35	0.12	18.86	0.92	0.85
48	73.23	5.62	31.59	1.46	0.33	0.11	19.40	3.14	9.84
49	67.53	3.86	14.88	1.44	0.26	0.07	19.85	0.81	0.66
50	70.52	5.12	26.22	1.58	0.40	0.16	19.02	1.20	1.44
51	72.88	8.41	70.68	1.26	0.19	0.04	19.87	1.01	1.02
52	73.80	4.38	19.16	1.52	0.41	0.17	20.91	0.78	0.60
53	73.50	5.54	30.69	1.43	0.27	0.07	19.70	0.81	0.66
54	72.29	3.84	14.74	1.84	0.69	0.47	19.36	1.05	1.10
55	71.59	6.64	44.14	1.51	0.35	0.12	18.74	0.91	0.82
56	73.56	6.72	45.22	1.46	0.33	0.11	22.76	1.04	1.07
57	70.11	5.94	35.32	1.44	0.26	0.07	27.58	0.86	0.74
58	72.74	5.88	34.58	1.59	0.40	0.16	19.65	0.89	0.79
59	73.70	7.02	49.21	1.26	0.19	0.04	19.37	1.56	2.43
60	70.81	9.25	85.58	1.52	0.41	0.17	19.70	0.91	0.83

X-Point #	Isolation			VSWR			Loss		
	$\bar{X}$	S	S^2	$\bar{X}$	S	S^2	$\bar{X}$	S	S^2
61	75.51	5.79	33.58	1.43	0.27	0.07	19.84	1.26	1.58
62	70.12	7.79	60.72	1.84	0.69	0.48	19.49	1.49	2.22
63	70.61	6.92	47.95	1.49	0.32	0.10	19.26	1.63	2.67
64	71.71	8.53	72.83	1.46	0.32	0.11	20.58	1.33	1.77
65	75.61	6.80	46.19	1.44	0.26	0.07	20.31	1.10	1.21
66	69.49	7.10	50.47	1.58	0.40	0.16	20.31	1.20	1.44

3.8 Task 8. Reliability Projections

Analysis and test plans to determine the reliability and life expectancy of a flight model were developed for the POC model and presented in the Task 8 Report. The qualification testing schedule for the RDX832 Dual-gate GaAs FET was included.

During the matrix development, the reliability analysis was updated to reflect circuit changes and to include recommended design modifications for flight hardware. The results are considered to be pessimistic since the matrix modeling is conservative. An exact mathematical model becomes very complex for a large matrix and was considered not to be cost effective at this time. The probability that a "fail-OFF" crosspoints occurs in 20 x 20 matrix for 10 years is 0.956026. The probability that a "fail-ON" crosspoint occurs in a 20 x 20 matrix for 10 years was estimated at 0.955060 for a flight model (MSM only). DCU reliability estimates are dependent on the type of memory devices which can be used for flight applications. The Failure Modes and Effects

Analysis have been completed and the results summarized in the Task 8 Report.

Reliability analysis was also performed for smaller size matrices including the 8 x 8 matrix included in the development plan for a Flight demonstration switch matrix system, Task 12.

3.9 Task 9. Product Assurance

A product assurance program was implemented in all development and fabrication phases for the breadboard and POC models. It included the final integration and the individual component module fabrication and testing. The quality assurance program was successful in insuring the integrity of the Proof-of-Concept model.

3.10 Task 10. Work Plan

The work plans identifying detailed subtasks required to accomplish all tasks were generated and updated during the development and fabrication of the switch matrix system.

3.11 Task 11. Reporting

Monthly technical reports on the performance analysis, financial status, task completion and problems were prepared between July 1980 and December 1982.

3.12 Task 12. Requirements Document and Development Plan for Flight Hardware.

A preliminary development plan for a flight demonstration switch matrix system has been conceived. It provided for one 8 x 8 engineering model switch matrix and three identical 8 x 8 switch matrix systems. It provided enough redundancy to achieve 0.97 probability of success for ten years of space operation. The tasks and cost breakdown structures have been included for a development and fabrication program scheduled for 28 months from commencement date.

An amended Task 12 was also completed in order to assist NASA in deriving overall spacecraft-system cost estimates earlier than previously anticipated. The task included final requirements document and development plan for flight hardware and the final development and test plan for flight hardware.

4. CONCLUSIONS AND RECOMMENDATIONS

The microwave switch matrix development program was concluded with the design, fabrication, and testing of a proof-of-concept (POC) 20 x 20 switch matrix model. This was the result of a two-year effort started with system architecture concept analysis, a study on the available present and future technology and continued with the development of the high speed switching circuit implemented in a 4 x 4 breadboard switch matrix.

This breadboard and the larger 20 x 20 POC switch matrix system proved with the present technology, the requirements for an advanced SS-TDMA communication system could be met or exceeded. The POC model demonstrated 15 ns switching speed, a 2.5 GHz bandwidth, and an outstanding routing capability. The POC model is considered to be ready for a flight demonstration program.

Larger switch matrices combining LSI/VLSI monolithic gallium-arsenide analog and digital circuits could be developed for 1987 technology. Integrated modules will be used as building blocks of the large matrix system. The performances should be comparable with the results obtained in the testing of the POC model.

Switching functions could be successfully combined on a single chip in the form of monolithic microwave circuit (MMIC) in which gallium-arsenide is not only the semi-insulating substrate but also can serve as the dielectric for microstrip or coplanar transmission lines.

The recommendations for future development efforts include:

- Qualification testing of the POC model

- Combine driver-and switch-amplifier modules into a single module to further improve the switching speed to less than 1 ns.

- Develop microwave switching techniques for frequencies to 20 GHz to simplify the 30/20 transponder design by eliminating the need for an IF frequency.

- Develop a monolithic crosspoint module for large microwave switch matrix systems (larger than 20 x 20).

The primary results which were drawn from the design and testing of the POC model are presented in the following paragraphs.

IF FREQUENCY

The IF frequency band was chosen to be 3.5 to 6.0 GHz with a center frequency of 4.75 GHz. This determination was made after an extensive analysis of the worst receive and transmit in-band spurious for an RF input frequency between 27.5 GHz and 30.0 GHz and for an output frequency between 17.7 GHz and 20.2 GHz. The results of this analysis are detailed in the Task 1 report, Sec 2.3.

ABSOLUTE MATRIX INSERTION LOSS

The insertion loss of any particular matrix path is determined by the total input and output coupler insertion losses and the corresponding switch amplifier gain. In addition to these individual components, the insertion loss can also vary slightly due to the interactions of these

individual components when they are interconnected in the matrix. The theoretical design dictates that if all switch-amplifiers have identical "ON" gain performance and each input-output coupler path pair have the same insertion loss, then the insertion loss for all matrix paths should be the same. In practice, however, there are many fabrication, assembly, and interconnect parameters that will influence the performance of any given path. To help account for these unknown effects, the switch-amplifier design included a final gain adjustment circuit that could help to compensate for insertion loss variations. By varying the bias conditions of the switch - amplifier, the "ON" gain could be adjusted by as much as $\pm$ 1.5 dB. This technique provided a large contribution when trying to equalize the matrix path insertion loss. Insertion loss results for the 20 x 20 switch matrix reveal an average insertion loss for all 66 crosspoints of 20.6 dB and a standard deviation of 1.6 dB. This includes only three crosspoints that were off from the average by more than 2.5 dB. Considering the complexity and size of the 20 x 20 switch matrix, these results are quite excellent and that the addition of the bias adjust on the switch-amplifier proved to be a successful technique to help attain these results.

PASSBAND RIPPLE AND BANDWIDTH

The frequency response curves shown reveal high passband ripple for the 20 x 20 switch matrix. The large variations in certain crosspoints are due to the interaction along the long rows of input and output couplers needed in the 20 x 20. This undesirable result was reduced for many crosspoints by doing some alignment in the tray. But for a few crosspoints, alignment proved to be only moderately successful. The

general bandwidth for all crosspoints is primarily determined by the bandwidth of the switch-amplifier which is 3.5 GHz to 6.0 GHz, but because of the coupler interaction ripple, the specification for 1 dB or 3 dB bandwidth must be revisited. The frequency response is not simply monotonic so that frequency response roll-off must be differentiated from in-band ripple. The basic conclusion of this discussion is that all crosspoints achieved a similar passband roll-off characteristic but certain units exhibited excessive ripple behavior over small sections of the passband. Several crosspoints did, however, achieve the entire 3.5 to 6.0 GHz frequency band with less than 3 dB ripple. Also the specification requiring a 1 GHz bandwidth with less than 1 dB ripple was met in several crosspoints.

ISOLATION

The isolation measurement is defined by taking the difference between the "ON" condition insertion loss and the "OFF" condition insertion loss. The signal level strength in the "OFF" condition can be separated into two different components. One component comes from the switch-amplifier "ON" to "OFF" isolation. This has been measured on every individual switch-amplifier prior to matrix integration and found always to exceed 70 dB. The second component can be described as physical isolation between the various microwave circuits. This type of isolation is determined by many factors such as the microwave circuit positioning in the tray as well as the cavities and paritions within the tray. Careful consideration was given to tray design which reduced this type of effect by providing adequate enclosure covers and isolation walls.

The results of the "ON" to "OFF" insertion loss test made on each matrix path was greater than 50 dB. This result tends to support that the dominate component in the isolation measurement is the physical isolation component. Additional tests were carried out using a spectrum analyzer that pointed out additional characteristics of the matrix. If two input signals at two different frequencies are applied to two adjacent input rows and only one crosspoint is turned "ON" a certain amount of the unwanted signal (indicated by the different frequency) will show up at the desired output port. In the worst case measured to date, this type of "isolation" was recorded at 40 dB. To help alleviate this type of problem in the future would require better physical isolation of the various microwave circuits.

VSWR

The input and output VSWR performance is influenced by many different components. The main contributor is the individual couplers themselves - each has an input and coupled port VSWR of between 1.05:1 and 1.4:1 depending on the frequency within the band. Then cascade 22 couplers together for both the input and output divider/combiner networks and the result can be a total VSWR variation of 1.1:1 to 2.0:1. Next add the input and output return loss of each switch—amplifier port compared to the 50 ohm load that is normally present during earlier testing and the VSWR can at some frequencies go as high as 3.0:1 especially in the frequency range from 5.5 GHz to 6.0 GHz. This type of poor VSWR ripple performance can be solved by several different techniques such as improved coupler design and switch - amplifier VSWR and/or the addition of properly placed isolation devices.

POWER TRANSFER CHARACTERISTICS AND PHASE LINEARITY

The power transfer and phase linearity of the switch matrix is a function of the switch-amplifier performance of these parameters. For the overall 20 x 20 matrix, the 1 dB compression point occurs at an input power level of 15dBm ± 1dBm depending on which crosspoint is evaluated. Phase shift at the 1 dB compression point is less than ± 3 degrees and at the 3 dB back-off is less than ±1 degree. Unless input power level requirements begin to approach the +15 dBm level, there should be no difficulty in meeting standard linearity specifications. In addition, the maximum allowable input power level for the 20 x 20 matrix should not exceed +25dBm at any time to insure matrix survival.

SWITCHING SPEED CHARACTERISTICS

The switching speed characteristic was measured on a sample of matrix crosspoints. The results show that the "ON" to "OFF" switching time was less than 10 nsec and usually about 6 nsec. The "OFF" to "ON" switching time was also less than 10 nsec and usually around 4 to 7 nsec. In all cases, the measured switching speed for either "ON" to "OFF" or "OFF" to "ON" will meet the 10 nsec requirement. Switching speed performance could be further improved by reducing the added capacitance used on each control gate of the dual-gate FET switching device. One other approach would be to improve the switching speed characteristics of the switch-driver circuit.

RECONFIGURATION RATE TESTS

Many tests were performed to demonstrate the many possible matrix state configurations. These tests included such examples as turning on one

crosspoint for a pre-set time period and then turning on a different crosspoint after a certain amount of dead time where no crosspoints were on. Other such examples involved several different crosspoints and many different state duration times. Tests were also performed to detail the signal propagation delay time variation when one crosspoint is turned off and another different path length crossoint is turned on. All crosspoints will change state at the same time if the data transfer pulse electrical length is varied according to the position of each crosspoint within the matrix. To eliminate this problem in the redundant paths is more complex and would require delaying the data transfer pulse at the DCU in some fashion. Without these types of improvements the worst case is a delay time of 15 nsec for a redundant path.

ROUTING TESTS

All primary and redundant paths were tested and found to provide 100% operation. In addition, several broadcast mode configurations were tested and the results are presented in the final matrix data section.

NASA CR-168175

SPACECRAFT IF SWITCH MATRIX FOR WIDEBAND SERVICE APPLICATIONS IN 30/20 GHz COMMUNICATION SATELLITE SYSTEMS

FINAL REPORT

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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15. Supplementary Notes

16. Abstract

The use of a dynamic switching matrix for future communication satellites will significantly increase the communication channel capacity and improve the system capability and flexibility.

This report describes the design and development of a unique coupler crossbar 20 x 20 microwave switch matrix. This report presents the test results of the proof-of-concept model that meets the requirements for a high-speed satellite switched, time division multiple access (SS-TDMA) system.

17. Key Words (Suggested by Author(s))		18. Distribution Statement
(SS-TDMA)	SATELLITE-SWITCHED, TIME DIVISION, MULTIPLE ACCESS	UNCLASSIFIED - UNLIMITED
POC	PROOF OF CONCEPT	
MSM	MICROWAVE SWITCH MATRIX	
DCU	DISTRIBUTION CONTROL UNIT	

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
UNCLASSIFIED	UNCLASSIFIED		

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CONTENTS

CONTENTS (Continued)

CONTENTS (Continued)

I. SUMMARY

I. SUMMARY

1.0 Final Report Contents

The Final Report includes an Executive Summary, which gives a brief overview of the program goals and objectives, along with a description of all twelve tasks performed for the NASA Switch Matrix Program. This section will highlight the 20 x 20 POC model details, including the basic requirements, description of the unit, and other aspects of the POC model program.

Section II will discuss in detail the design of each POC model component. In addition, the matrix integration will also be outlined. The third section will present sufficient POC model test data to describe the performance of the unit. Section IV will analyze the data obtained on the POC model with respect to certain key parameters. Critical assessment of the POC model will be discussed in Section V along with recommendations for future matrix improvements. Finally, in Section VI, the matrix reliability question will be addressed.

2.0 MATRIX REQUIREMENTS

The required specifications for the 20 x 20 switch matrix are completely outlined in Fig. 2.1 of Section III. Some of these specifications which were more critical than others and directly impacted the POC design are switching speed, IF bandwidth, insertion loss, input and output VSWR, isolation, passband ripple, and DC power. To meet the required specifications often required trade-offs between

parameters and frequently compromised the optimum overall performance.

3.0 DESCRIPTION OF POC MODEL

The 20 x 20 POC model switch matrix consists of two major functional blocks. The first block is the microwave switch matrix portion consisting of two individual sub-assemblies which are bolted together and interconnected by semi-rigid microwave coax cable to form the complete 20 x 20 microwave switch matrix. The matrix design is referred to as coupler crossbar architecture and its specific advantages are outlined in Section II, Part 1.0 of the POC model design section. The main switching element in the matrix, the switch amplifier, uses a two-stage dual-gate GaAs FET operating in a gain mode as the switching element. This particular design approach not only provides good isolation and switching speed, but also provides gain in the ON switch position. The switch control voltage required by the switch-amplifier is provided by a thick-film hybrid high-speed driver circuit. All matrix components are individually tested and then integrated into the multi-layer tray configuration. The 20 x 20 POC model switch matrix is partially populated and includes seventy-six active crosspoints out of the possible 484 possible locations. Two additional paths are included to provide wraparound redundancy.

The second major block is the distribution control unit (DCU). The DCU exercises a preprogrammed memory to control each individual crosspoint within the microwave switch matrix. The DCU contains many different circuit blocks mounted into standard breadboard wire-wrap type circuit boards. The unit is housed in an aluminum enclosure with a clear plastic cover so that LED display segments can be viewed during DCU operation. A standard keyboard is also included to load

ROM memory with various switch matrix configurations. The DCU is interconnected to the microwave switch matrix via six 100-wire cable assemblies.

4.0 POSITIVE HIGHLIGHTS OF THE 20 X 20 POC MODEL

The 20 x 20 POC model has successfully demonstrated that coupler crossbar architecture is an outstanding approach for SS-TDMA type microwave switching. The POC model demonstrated wide bandwidth (2.50 GHz), low insertion loss (approximately 20 dB) and very fast ON/OFF switching speed (less than 5 nsec). The DCU provided a variety of TDMA testing examples that demonstrated beyond any doubt the TDMA capability of the POC model. The 20 x 20 POC model mechanical design was packaged to yield reasonable size and weight for the microwave switch matrix.

5.0 FABRICATION AND ASSEMBLY

The fabrication and assembly of the 20 x 20 POC model was a major feat in itself. The fabrication task included over 500 thin-film MIC coupler substrates, 37 thin-film MIC amplifier substrates, 74 thick-film driver and bias substrates, and 13 PC driver and data transfer board assemblies. Over 700 glass to metal feed-thrus were installed in the switch amplifier modules and the matrix tray. The top and bottom trays were individually assembled and tested, then interconnected and tested again. To do any work on either tray involved using a specially designed heated station that incorporated 4 large heating elements. Bonding of the coupler substrates was also difficult in certain tray locations due to limitations of some existing equipment. The assembly techniques developed for this program will provide

insight for future designs when the tray size is large and complicated.

6.0 PROBLEMS

The problems encountered (and solved) in the production of the 20 x 20 switch matrix were primarily due to the large physical size and complexity of the matrix package. As reported in the previous paragraph, the large quantities of parts to be assembled posed additional problems. This was most evident in the coupler substrate installation. Each coupler substrate was adhesively attached using a conductive silver epoxy pre-form. One or two rows of couplers were installed at a time using specially developed assembly fixtures. The silver epoxy was then cured for several hours at an elevated temperature. Since the chassis was not gold plated, the heating and cooling process accelerated the formation of an oxide layer on the aluminum chassis in the rows where couplers were still not installed. The resulting oxidation increased the RF ground path resistance and, therefore, degraded the performance of certain coupler rows. Other problems associated with the installation of the switch amplifier module and bias circuit, the driver circuit PC boards, the RF and DC feedthrus were adequately resolved for the POC model with no impact on performance or reliability of the matrix.

Electrical performance problems were also encountered which were related to the complexity and size of the POC model. The long rows of couplers used on the matrix introduced unexpected VSWR interaction as well as line losses which increased the insertion losses beyond that which was predicted. Part of these problems was a result of the oxidation problem mentioned earlier, and part was due to the under-

estimation of the VSWR interaction associated with such long rows of couplers. The variation in isolation between adjacent and non-adjacent crosspoints also occurred indicating that even though cavity isolation was included wherever possible, that further study is needed to assure that adjacent crosspoints are guaranteed maximum physical isolation. In general, nearly all the fabrication, process, and assembly problems were adequately solved at the engineering level during the POC model program. This conclusion is based on the outstanding performance achieved by the 20 x 20 POC model.

II. POC MODEL DESIGN

SECTION II

20x20/22x22 POC IF SWITCH MATRIX DESIGN

The IF Switch Matrix design is handled by considering the system and composed of two basic building blocks: (1) the IF signal propagation and switching system (referred to as the Switch Matrix) and (2) the digital and control logic system (referred to as the Distribution Control Unit (DCU). These two building blocks are shown in Figure 1.1 and will be discussed separately.

1.0 IF SWITCH MATRIX SIGNAL SYSTEM DESIGN - COUPLER CROSSBAR ARCHITECTURE

For the 20 x 20 IF switch matrix design, the IF signal propagation and switching is handled by coupler-crossbar architecture. This type of architecture presents many advantages (see Task 1 Final Report NASA #1-5--F-1-T1/WDL #TR 9085) including electrical and mechanical parameters, reliability, redundancy, flexibility and an outstanding broadcast mode of operation. The advantages of the coupler-crossbar switch matrix architecture are the following:

- Planar structure offering good compactness (least volume, size and weight)
- Easy to manufacture by partitioning the system into small identical submodules
- Enhanced reliability due to:
  - Minimum number of switching devices per crosspoint are used:
  - A failed switching element has little effect on the overall system performance since reflected power is absorbed in the coupler load
- Redundancy is simplier to implement than other architectures

IF SWITCH MATRIX SYSTEM

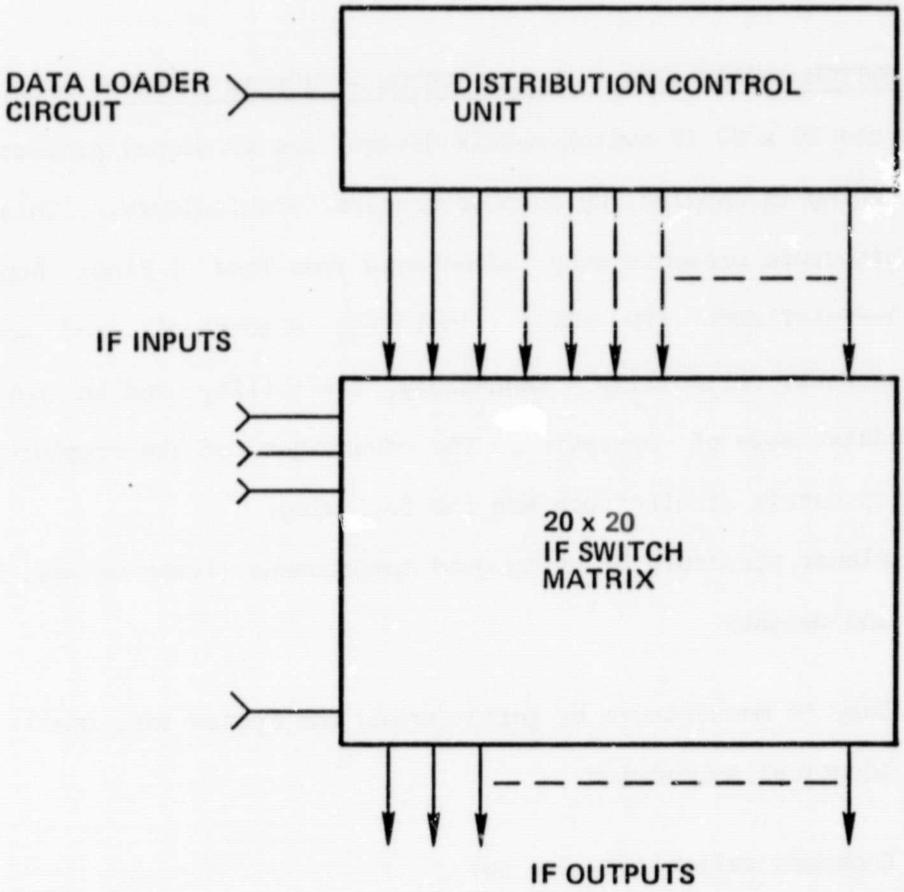

Fig. 1.1

by using wraparounds (e.g. SPMT architecture)

- Reliability can be easily increased through the use of wraparounds
- The output signal level is independent on the communication path
- Broadcast mode of operation is a built-in capability of the coupler crossbar architecture, with no overall performance degradation
- The system is easier to match than other system architectures

The coupler-crossbar IF switch matrix architecture concept is presented in Fig. 1.2. Directional couplers are used between the input lines of the matrix and each crosspoint switch- amplifier within the matrix. The design is established so that the power level at every switch input is always equal. After switching and amplification, the IF signal is connected to the desired output line of the matrix through an output directional coupler such that the power level at all output ports of the IF switch matrix is always equal and independent of the signal path through the matrix. The coupling coefficient of input/output directional couplers depends on the crosspoint location in the matrix. Twenty-two (22) different coupling coefficients are needed for the 484 input and 484 output couplers of a complete 22 x 22 IF switch matrix.

The block diagram of a 20x20 IF switch matrix system including two redundant signal paths is presented in Fig. 1.3 . The insertion loss of the IF switch matrix, independent of the signal path, is a function of the coupling coefficients of the input and output couplers and the gain of the switching amplifier connected between the input

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20 X 20 IF SWITCH MATRIX USING COUPLER CROSSBAR ARCHITECTURE

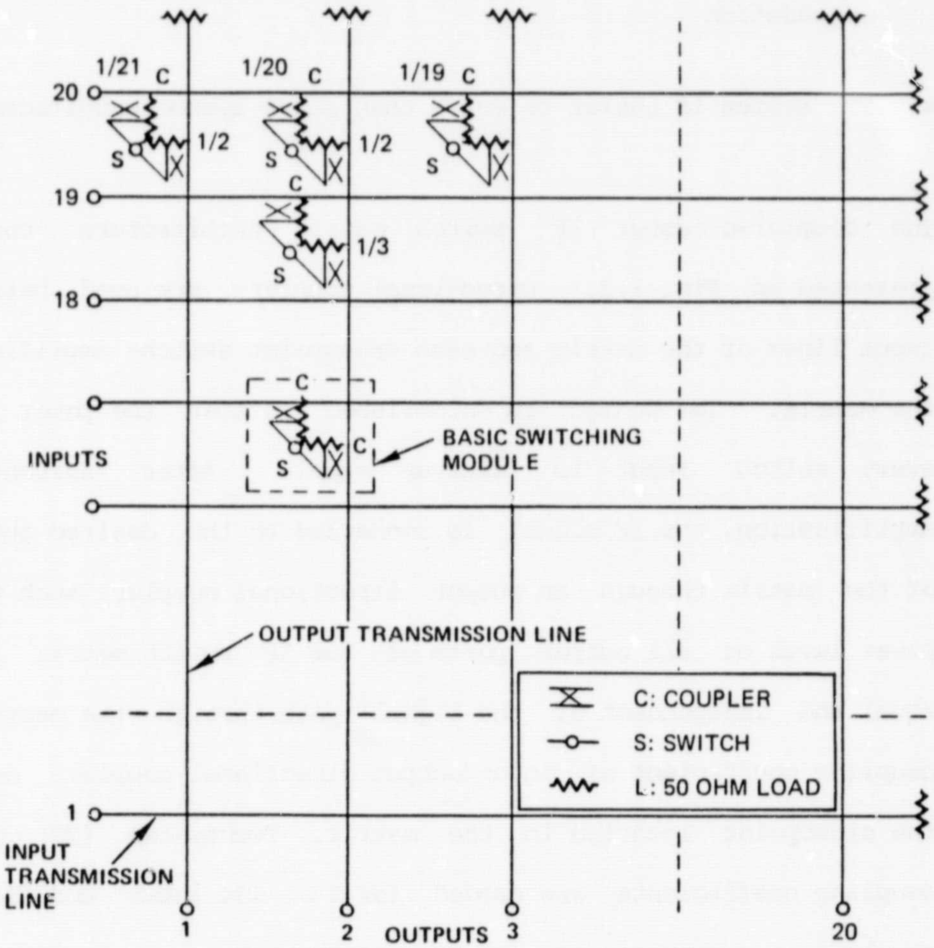

Fig 1.2

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IF SWITCH MATRIX

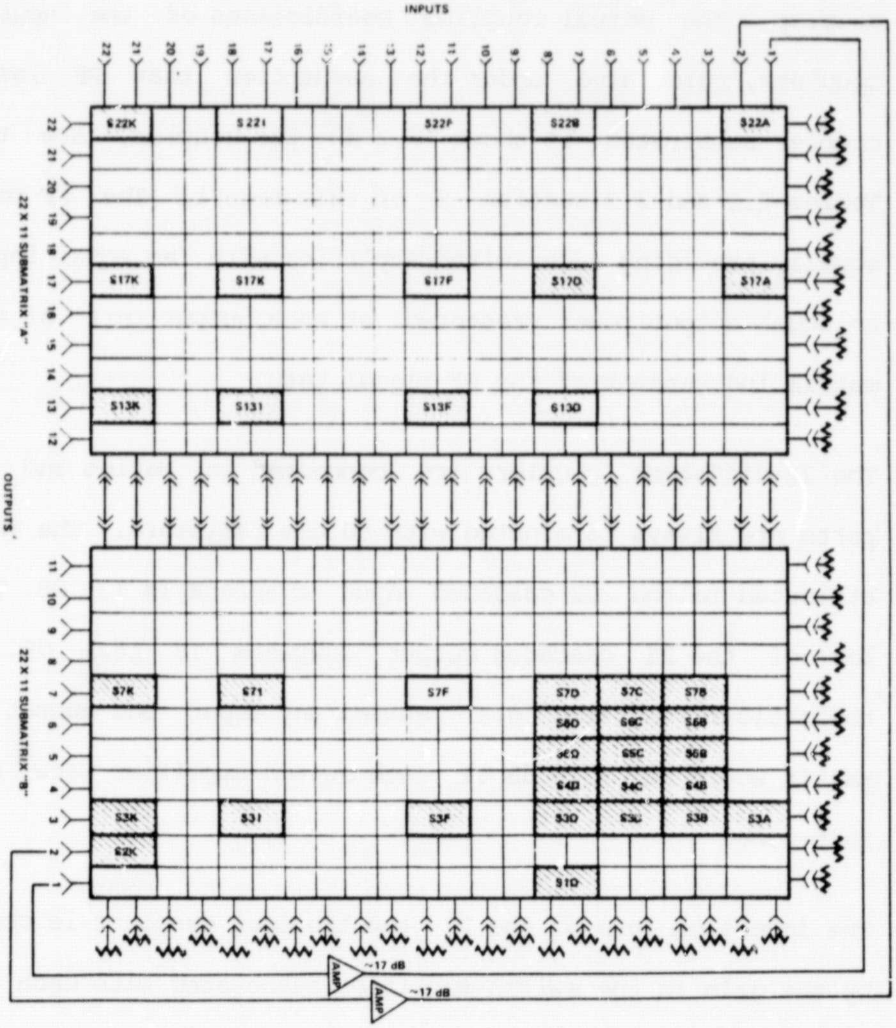

Fig. 1.3

and output couplers. The coupling coefficient of two adjacent couplers on the same row or column of the matrix is given by:

$$1/K_{n+1}=1/(K_n+1)$$

Assuming the coupling coefficient of the last coupler being 1/3, the coupling coefficients of the next couplers will be 1/4, 1/5, 1/6 thru 1/24. We selected 1/3 as the coupling coefficient of the first coupler. The actual coupling coefficients of the input and output couplers, calculated under the assumption that RF losses in the coupler substrates is about 0.2 dB per coupler, are tabulated in Tables 2.1 and 2.2 section 2 of this report. The RF power is split equally providing each switch-amplifier with an equal input power and an equal output power presented at each output port of the IF switch matrix independent of the RF signal path.

The 22 different couplers are connected in series and the isolated ports are always terminated with 50 ohm resistors. The insertion loss atributed to the 22 cascaded input couplers is 17 dB. The insertion loss of the 22 cascaded output couplers is 16.5 dB. The total theoretical insertion loss between any input and output port of the matrix would be 33.5 dB if each switch-amplifier were replaced by a thru-line.

The insertion loss of the 22 input/output couplers is compensated for by the gain in the switch-amplifier associated with each crosspoint of the matrix and is estimated to be 16 dB minimum. If no additional losses are present in the actual matrix layout, there are no difficulties in meeting the specification requirement of maximum 18 dB for the insertion loss of the matrix. In a larger matrix, this specification requirement could be marginal, since in this case the same input power must be split equally to a higher number of coupled ports of the

matrix.

Switching speed performances of the IF switch matrix system are primarily governed by the switch driver module response characteristics since the switching speed of the dual-gate GaAs FETs is much less than 1 ns. The specifications and capabilities of individual subsystems and modules will be analyzed in the corresponding sections of this report.

The block diagram presented in Figure 1.4 shows the 20x20/22x22 switch matrix partitioned in two submatrices of size 22x12 and 22x10 which are interconnected and folded-over to obtain the full 22 x 22 matrix. One switch-amplifier and one switch driver module are necessary for each set of two adjacent crosspoints of the matrix.

Associated with each set of two adjacent crosspoints of the matrix are the following subassemblies:

1. Input coupler substrate, 2 (ea)
2. Switch-amplifier module, 1 (ea)
3. Switch-driver module, 1 (ea)
4. Output coupler substrates, 1 (ea)

The proof-of-concept model for a 20x20/22x22 matrix is not fully populated with the active circuits or modules for each of the 484 crosspoints. Only 66 active crosspoints have been included into basic 20x20 switch matrix and 10 active crosspoints in the wraparound redundant signal path. The location of these 76 active crosspoints of the matrix were selected to evaluate switching capability throughout the matrix. The active switch matrix consists of 12 input ports and 8 output ports.

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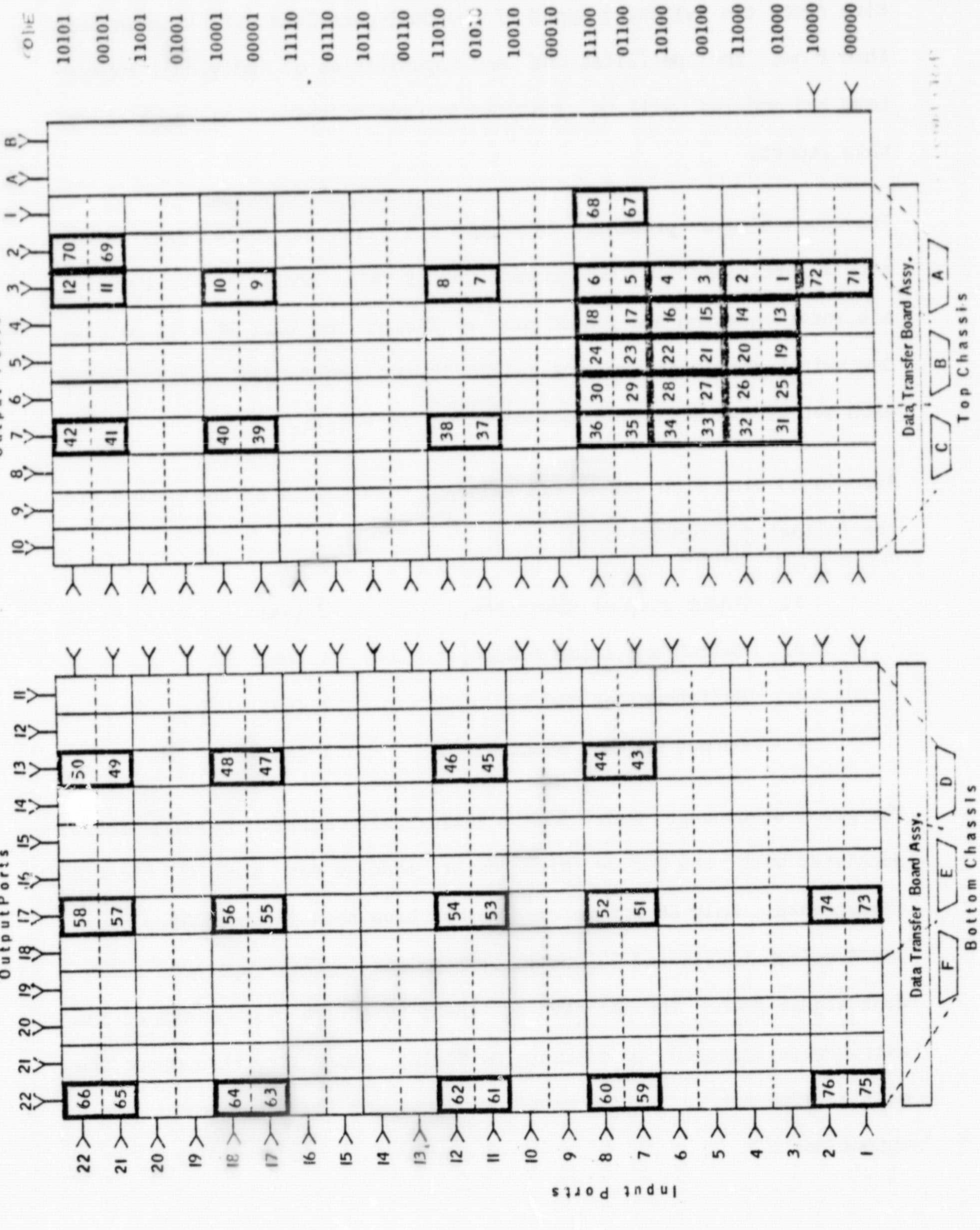

Fig. 1.4 Crosspoint Locations

In this configuration, 10 redundant crosspoints of the matrix provide wraparound capability for 12 crosspoints.

Figure 1.4 shows the location of the 66 active crosspoints numbered from 1 to 66 and the 10 redundant crosspoints number 67 to 76.

Crosspoints 1 thru 66 are part of the basic 20x20 matrix and crosspoints 67 thru 76 are included in the redundant path. Only crosspoint #'s 5, 6, 11, 12, 51, 52, 57, 58, 59, 60, 65 and 66 are provided with the redundant path capability.

2.0 INPUT AND OUTPUT COUPLER DESIGN

2.1 Requirements

One of the requirements of the input and output couplers is that at center frequency the coupled loss is the determined theoretical value (see Table 2.1 and 2.2). The theoretical coupling coefficients are selected such that equal signal RF power is available at all 22 coupled ports of 22 series connected couplers.

Another requirement is that individual VSWR should be less than 1.2:1 and series cascaded VSWR should be less than 1.5:1.

For coupling coefficients tighter than -9 dB, Lange interdigitated couplers are used for both input and output couplers. Side by side couplers are used for coupling coefficients less than -9 dB.

The POC model is only partially populated with input/output couplers. Couplers are installed only in rows or columns where an active crosspoint exists (see Fig. 2.1 and 2.2)

Table 2.1

NASA 22x22 Microwave Switch Matrix Input Couplers Dimensions

Theoretical Coupling Coefficient (dB)	Drawing No.	Width (mils)	Spacing (mils)	Length (mils)
4.8	SKEB-N5201-01N1	2.20	4.50	240
6.2	SKEB-N5202-01N1	2.40	7.15	240
7.5	SKEB-N5203-01N1	2.60	9.70	240
8.4	SKEB-N5204-01N1	2.70	11.60	240
9.2	SKEB-N5205-01N1	19.048	5.458	220
9.9	SKEB-N5206-01N1	19.718	6.646	220
10.6	SKEB-N5207-01N1	20.297	7.926	220
11.2	SKEB-N5208-01N1	20.728	9.095	220
11.7	SKEB-N5209-01N1	21.047	10.117	220
12.2	SKEB-N5210-01N1	21.332	11.177	220
13.1	SKEB-N5211-01N1	21.772	13.180	220
13.5	SKEB-N5212-01N1	21.940	14.110	220
13.9	SKEB-N5213-01N1	22.096	15.058	220
14.3	SKEB-N5214-01N1	22.235	16.035	220
14.7	SKEB-N5215-01N1	22.364	17.026	220
15.1	SKEB-N5216-01N1	22.481	18.043	220
15.4	SKEB-N5217-01N1	22.561	18.815	220
15.7	SKEB-N5218-01N1	22.637	19.600	220
16.1	SKEB-N5219-01N1	22.730	20.665	220
16.4	SKEB-N5220-01N1	22.794	21.476	220
16.7	SKEB-N5221-01N1	22.853	22.300	220
17.0	SKEB-N5222-01N1	22.909	23.135	220

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Table 2.2

NASA 22x22 Microwave Switch Matrix Output Couplers Dimensions

Substrate size: 1.445" x 0.350" x 0.025"
Loss: 0.2 dB per coupler (Two couplers on each substrate).
Qty : 10 of each type, total 110 substrates
70(ea) installed on columns 1,2,3,4,5,6,and 7, top 22x10 submatrix
40(ea) installed on columns 13,17,and 22, bottom 22x12 submatrix

Theoretical Coupling Coefficient (dB)	Drawing No.	Width (mils)	Spacing (mils)	Length (mils)
4.8 & 6.2	SKEB-N5231-01N1	2.20	4.50	240
		2.40	7.15	240
7.4 & 8.3	SKEB-N5232-01N1	2.60	9.70	240
		2.70	11.60	240
9.1 & 9.8	SKEB-N5233-01N1	18.943	5.298	220
		19.629	6.470	220
10.4 & 11.0	SKEB-N5234-01N1	20.140	7.553	220
		20.590	8.700	220
11.5 & 12.0	SKEB-N5235-01N1	20.925	9.703	220
		21.222	10.749	220
12.5 & 12.9	SKEB-N5236-01N1	21.489	11.832	220
		21.682	12.726	220
13.4 & 13.8	SKEB-N5237-01N1	21.900	13.875	220
		22.058	14.820	220
14.1 & 14.5	SKEB-N5238-01N1	22.167	15.544	220
		22.301	16.530	220
14.8 & 15.2	SKEB-N5239-01N1	22.359	17.280	220
		22.508	18.300	220
15.5 & 15.8	SKEB-N5240-01N1	22.587	19.075	220
		22.661	19.865	220
16.2 & 16.5	SKEB-N5241-01N1	22.751	20.934	220
		22.814	21.752	220

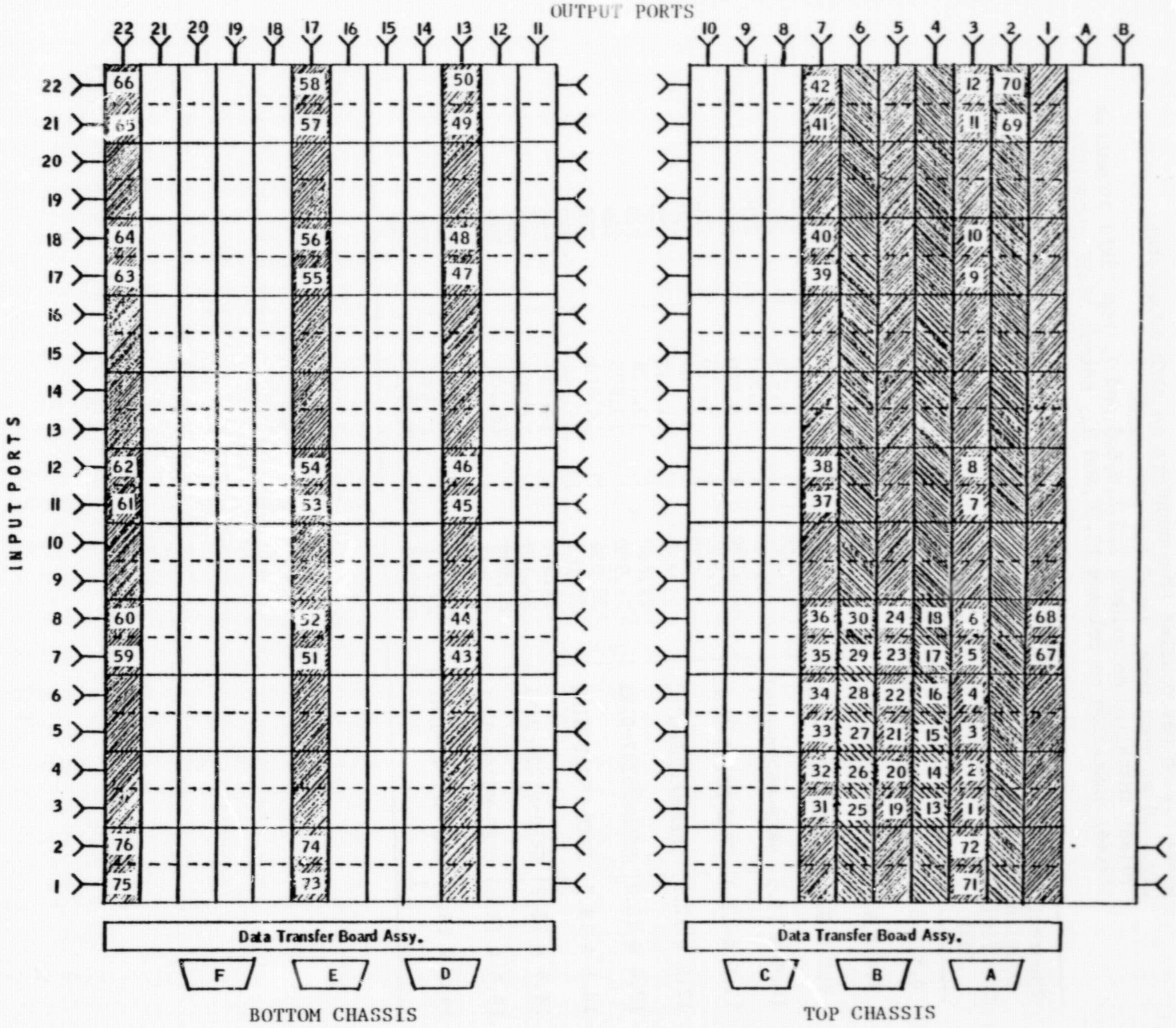


Fig. 2.1 Output Coupler Locations

C-2

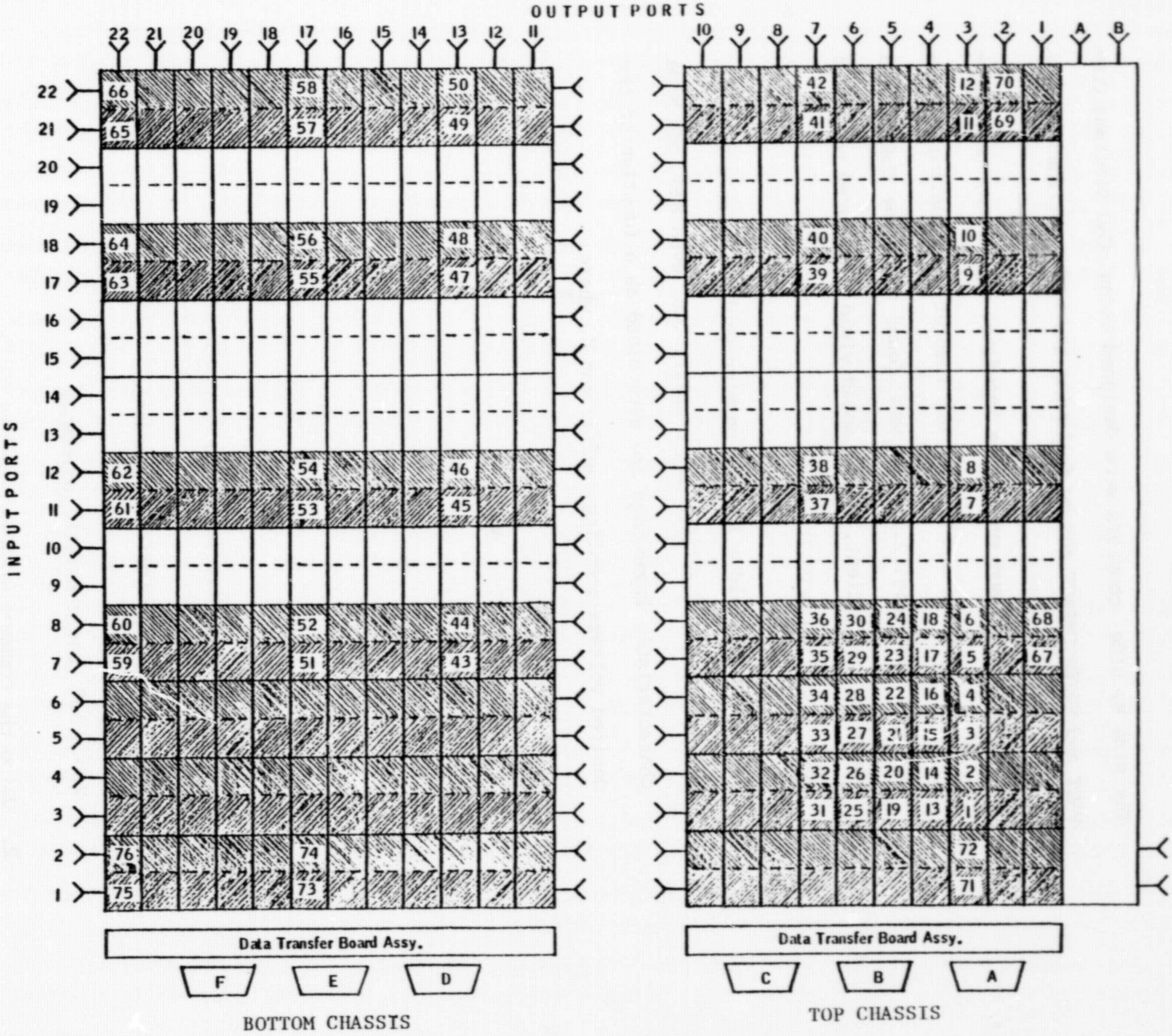


Fig. 2.2 Input Coupler Locations

2.2. Design Approach

A) Side-by-Side Couplers

The side by side couplers were designed using CAD programs COMPACT and SUPERCOMPACT and by following the steps outlined below.

1. Using the odd and even mode impedance equations, we determined unique Zoe and Zoo for our theoretical coupling coefficient. (See Fig. 2.3) It was found that the theoretical coupling coefficient, (K dB) would yield a measured result of (K + 0.2) dB.

   Therefore to yield a 17.0 dB coupler would require a Zoo, Zoe determination on a 16.8 dB coupler. The even and odd mode characteristic impedances are determined as a function of the desired voltage coupling coefficient K, where

   $$K = \frac{Zoe - Zoo}{Zoe + Zoo} \quad \text{and}$$

   $$Z_o^2 = Zoe \times Zoo$$

   and

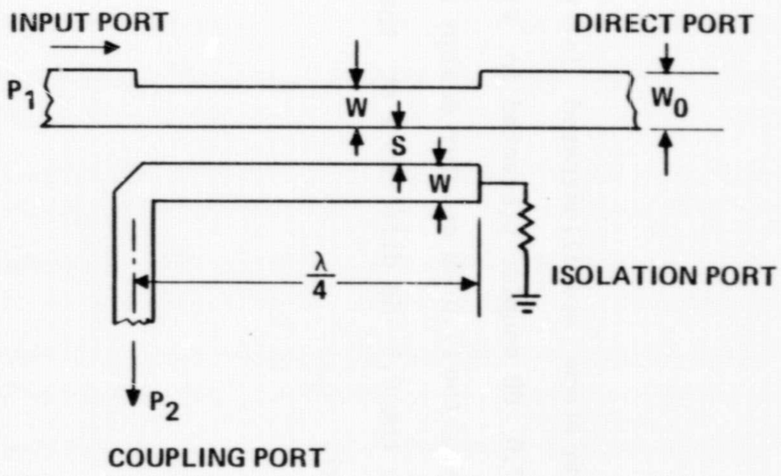
   Zo = characteristic impedance

   Zoe = even characteristic impedance

   Zoo = odd characteristic impedance

2. Using the COMPACT program TRLINES, we determine the physical width and spacing of the coupler at the center frequency. By

SIDE BY SIDE COUPLER DESIGN



- LENGTH DETERMINED AT CENTER FREQUENCY (4750 MHz)

$$L = \lambda/4 \qquad \text{AND} \qquad \lambda = \frac{\nu}{f\sqrt{E_{eff}}}$$

ν = PROJECTION VELOCITY

= 3×10^{10} cm/sec.

f = FREQUENCY IN Hz

= 4750×10^6

ϵ_{eff} = EFFECTIVE DIELECTRIC INSTANT

Fig. 2.3

using an interactive method, the exact odd and even characteristic impedances Zoo and Zoe are defined.

3. By experimentation, we found the SUPERCOMPACT program will be 0.3 dB off from the actual measured coupler. Therefore a 17.0 dB coupler design analyzed on SUPERCOMPACT will yield an analyzed center frequency coupling coefficient of 16.7 dB.

   Example:

   Actual desired coupling coefficient = 17.0 dB

   Theoretical coupling analysis target = 16.8 dB

   Zoe = 57.835

   Zoo = 43.227

   W = 22.909 MILS

   S = 23.135 MILS

   The coupler design steps are illustrated in the computer printouts for a 17.0 dB coupler presented in Fig. 2.4. The frequency response of the 17.0 dB coupler design is also shown in Fig. 2.4 (Note the 0.3 dB difference at the center frequency of 4.75 GHz).

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Computer Aided Coupler Analysis

```
* C TEST.
BLK
  CPL 1 2 3 4 W=22.909MIL S=23.135MIL PLEN=240MIL ALUM
  RES 2 0 R=50
  RES 4 0 R=50
  CUP: 2POR 1 3
END
FREQ
  ?750MHZ
END
OUT
  PRI CUP 3 R1=50 R2=50
END
DATA
  ALUM: MS H=25MIL ER=10.2 MET1 CR 304A MET2 CU 31750A MET3 AU 17780A
END
```

```
* COMPACT

COMPACT VERSION 5.1 + 59 - IMPLEMENTED 12/11/80
SEE NEWS FOR FIVE NEW FEATURES PLUS LANGE COST SAVING HINTS

FILE NAME, 'TRXINFO', 'TRLINES', 'LANGE', 'NEWS' OR 'QUIT'?TRLINES
BRYANT-WEISS OR APPROXIMATE SOLUTION (BW/A)?BW
MICROSTRIP, SHIELDED MICROSTRIP OR QUIT (MS/SH/QU)?MS
ENTER SINGLE OR COUPLED LINES (S/C)?C
NO. SUBSTRIPS PER STRIP (25 MAXIMUM)?25
ENTER RELATIVE DIELECTRIC CONSTANT?10.2
UNITS: ENGLISH, METRIC OR RATIOS (E/M/R)?E
SUBSTRATE THICKNESS(MILS)?25
WIDTH(MILS): ENTER START, STOP AND STEPSIZE?22.909
SPACING(MILS)?23.135

   COUPLED STRIPS      SPA = 23.135 MILS      K = 10.20

     W          ZOE     ZOO           VE       VO         KEFFE   KEFFO
    MILS            OHMS              E+08 M/SEC
  22.909      57.835  43.227      1.105    1.221        7.360   6.028

MICROSTRIP, SHIELDED MICROSTRIP OR QUIT (MS/SH/QU)?QU
FILE NAME, 'TRXINFO', 'TRLINES', 'LANGE', 'NEWS' OR 'QUIT'?QUIT
* DONE
```

```
* SCOMPACT

SUPER COMPACT  Version 1.5+15  11/09/81      18-MAR-82  09:09:43

CMD > TEST.
CMD > ANA

CIRCUIT:  CUP
S-MATRIX, ZS =   50.0+J   0.0  ZL =   50.0+J   0.0

  FREQ          S11            S21            S12            S22          |S21|  STAB SGN
  GHz        MAG    ANG     MAG    ANG     MAG    ANG     MAG    ANG      db        K  B1
  2.00000   0.003   -67   0.091    52   0.091    52   0.003   -67   -20.85   60.85 +
  2.25000   0.004   -71   0.100    47   0.100    47   0.004   -71   -20.01   50.13 +
  2.50000   0.005   -76   0.108    42   0.108    42   0.005   -76   -19.30   42.56 +
  2.75000   0.006   -81   0.116    38   0.116    38   0.006   -81   -18.70   37.06 +
  3.00000   0.007   -86   0.123    33   0.123    33   0.007   -86   -18.19   32.99 +
  3.25000   0.008   -91   0.129    28   0.129    28   0.008   -91   -17.77   29.95 +
  3.50000   0.009   -97   0.134    24   0.134    24   0.009   -97   -17.43   27.67 +
  3.75000   0.010  -102   0.139    19   0.139    19   0.010  -102   -17.16   25.98 +
  4.00000   0.011  -108   0.142    14   0.142    14   0.011  -108   -16.95   24.77 +
  4.25000   0.013  -114   0.144     9   0.144     9   0.013  -114   -16.81   23.97 +
  4.50000   0.014  -120   0.146     5   0.146     5   0.014  -120   -16.72   23.51 +
  4.75000   0.015  -126   0.146     0   0.146     0   0.015  -126   -16.70   23.39 +
  5.00000   0.016  -132   0.146    -5   0.146    -5   0.016  -132   -16.74   23.59 +
  5.25000   0.017  -139   0.144    -9   0.144    -9   0.017  -139   -16.84   24.13 +
  5.50000   0.019  -145   0.141   -14   0.141   -14   0.019  -145   -17.00   25.04 +
  5.75000   0.020  -152   0.138   -19   0.138   -19   0.020  -152   -17.22   26.37 +
  6.00000   0.021  -159   0.133   -23   0.133   -23   0.021  -159   -17.52   28.21 +

PLOT, PRINT OR QUIT? (PL/PR/<Q>): Q
CMD > END

*** END SUPER COMPACT ***
```

Fig. 2.4

B) Lange (Interdigitated) Couplers

A computer program designed by COMPACT computes Lange coupler parameters and was used in the design of these couplers. Through experience, it has been found that the actual coupling is .1 dB higher than the COMPACT design. Also, the actual center frequency is about 250 MHz lower than COMPACT design. Knowing these trends, we can optimize the compact program to get our desired result. The design procedure and equations for Lange couplers are presented in Fig. 2.5.

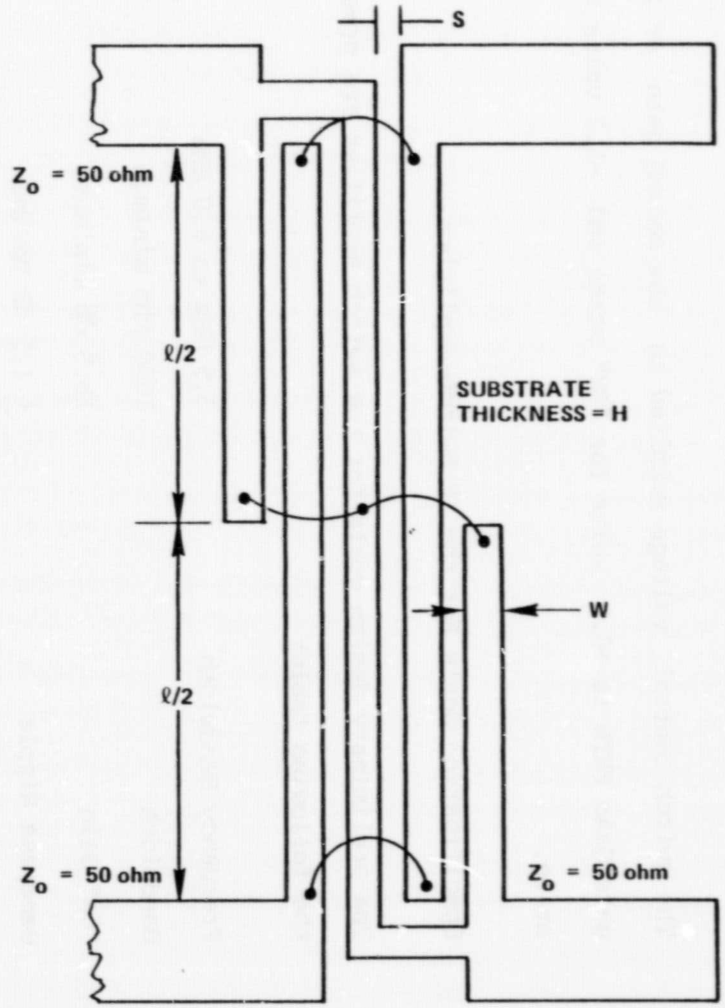
2.3. Coupler Fabrication

There are two different couplers being manufactured; input and output. Both are manufactured the same way but on different size substrates. The input coupler dimensions are 1.410" x .250" x .025". The output coupler dimensions are 1.445" x .350" x .025", with two adjacent couplers etched on each substrate. The weight of an input coupler is .67 grams and the weight of an output coupler is .86 grams.

The couplers are manufactured on Alumina substrates with a Chrome-Copper-Gold metalization. The couplers are drawn 10 to 1 or 40 to 1, and a Rubylith is cut to dimensions. A glass mask at the scale 1:1 is shot or through an intermediate step. The coupler substrates are etched in-house using the ion mill etching process. The resultant coupler size and dimensions are very close to the expected values and the electrical performance is repeatable for all couplers used in the switch matrix assembly.

Tables 2.1 and 2.2 present the calculated dimensions of 22 input and output couplers used for the IF Switch Matrix.

DESIGN EQUATIONS FOR INTERDIGITATED COUPLER



$$Y_o^2 = \frac{\left[(K-1)\,Y_{oo}^2 + Y_{oo}Y_{oe}\right]\left[(K-1)\,Y_{oe}^2 + Y_{oo}Y_{oe}\right]^2}{(Y_{oo} + Y_{oe})^2}$$

$$C = \left[\frac{(K-1)\,Y_{oo}^2 - (K-1)\,Y_{oe}^2}{(K-1)\,Y_{oo}^2 + 2\,Y_{oo}Y_{oe} + (K-1)\,Y_{oe}^2}\right]$$

WHERE

Y_o	IS THE CHARACTERISTICS ADMITTANCE OF THE SYSTEM
K	IS THE NUMBER OF THE INTERDIGITATED FINGERS
C	IS THE DESIRED POWER COUPLING COEFFICIENT
Y_{oe}	IS THE EVEN MODE ADMITTANCE OF THE COUPLED LINE
Y_{oo}	IS THE ODD MODE ADMITTANCE OF THE COUPLED LINE

A COMPUTER PROGRAM "LANGE" HAS BEEN WRITTEN TO CALCULATE THE EVEN MODE AND ODD MODE IMPEDANCES OF THE INTERDIGITATED COUPLER WITH ANY DESIRED COUPLING COEFFICIENTS.

Fig. 2.5

Layout examples of interdigitated (Figure 2.6) and side-by-side couplers (Figures 2.7 and 2.8) are presented. The layout of each coupler includes sections of 50 ohm transmission lines of different lengths. This way, when 22 couplers are series connected, the effect of the reflected signals will not be cumulative at the same frequency. The return loss ripple will be spread more or less equally inside the frequency band of 3.5 GHz to 6.0 GHz.

3.0 IF SWITCH AMPLIFIER MODULE

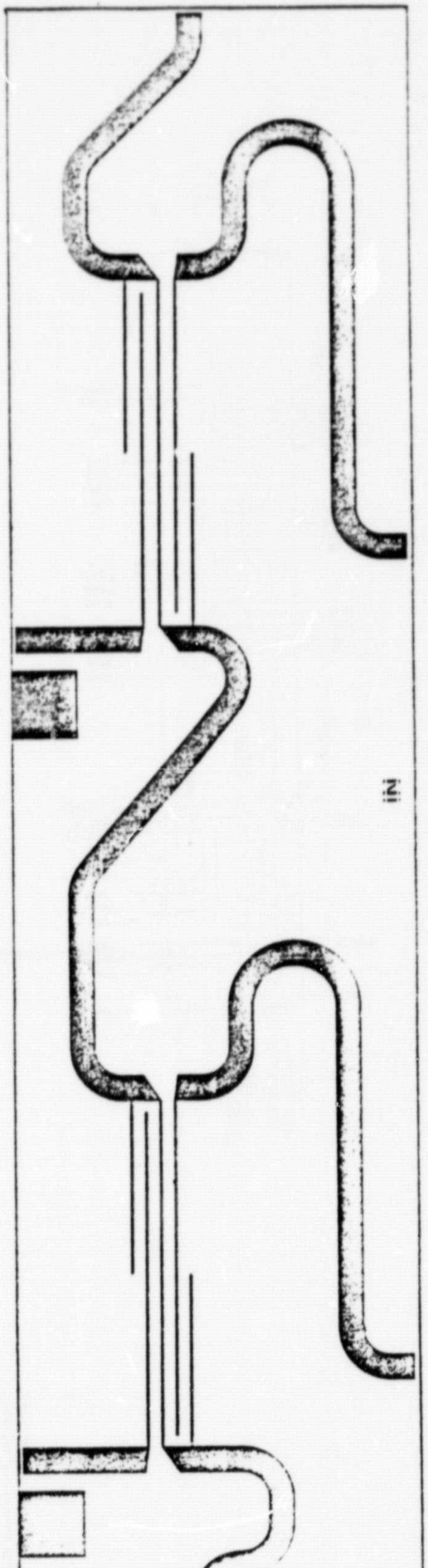
The block diagram of the switch amplifier module in Fig. 3.1 presents the circuits needed for two adjacent crosspoints of the matrix. An adjustable biasing voltage for gate-1 of the dual-gate GaAs FETs is supplied to each crosspoint switch-amplifier from an external adjustable DC source. This external voltage is used to set the insertion loss of each crosspoint to the specification value.

The switch control voltage supplied to the second gate of the dual-gate GaAs FETs is +0.2 volts for "ON" state and -5.2 volts for "OFF" state.

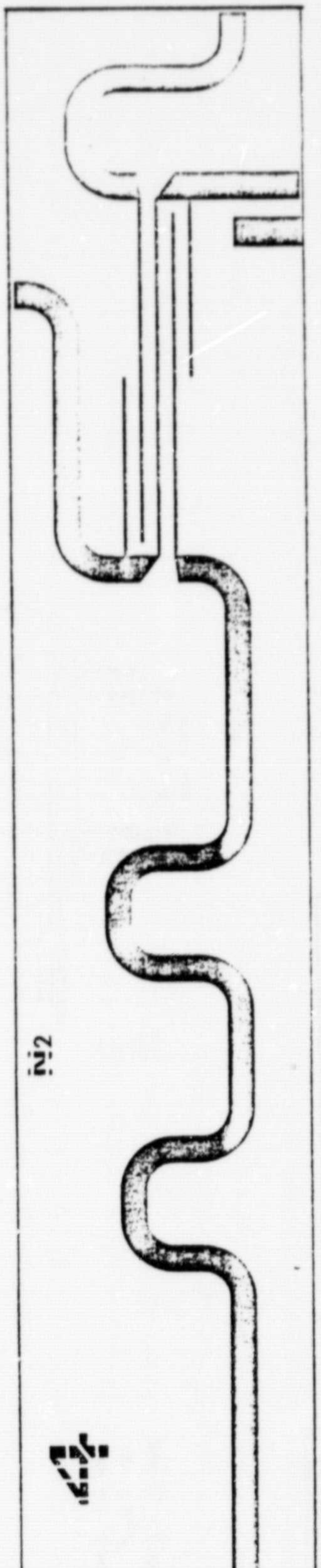
3.1 Specification Goals For the IF Switch-Amplifier

The preliminary design goals for the switch amplifier are presented in the following table:

Frequency Bandwidth	3.5 GHz to 6.0 GHz
Bandwidth	1000 MHz minimum
"ON" Gain	15.5 dB minimum
Bandpass Ripple	± 1.5 dB maximum
"ON" to "OFF" Isolation	53 dB Minimum



Dual Output Lange Interdigitated Coupler Layout



Input Lange Interdigitated Coupler Layout

Fig. 2.6

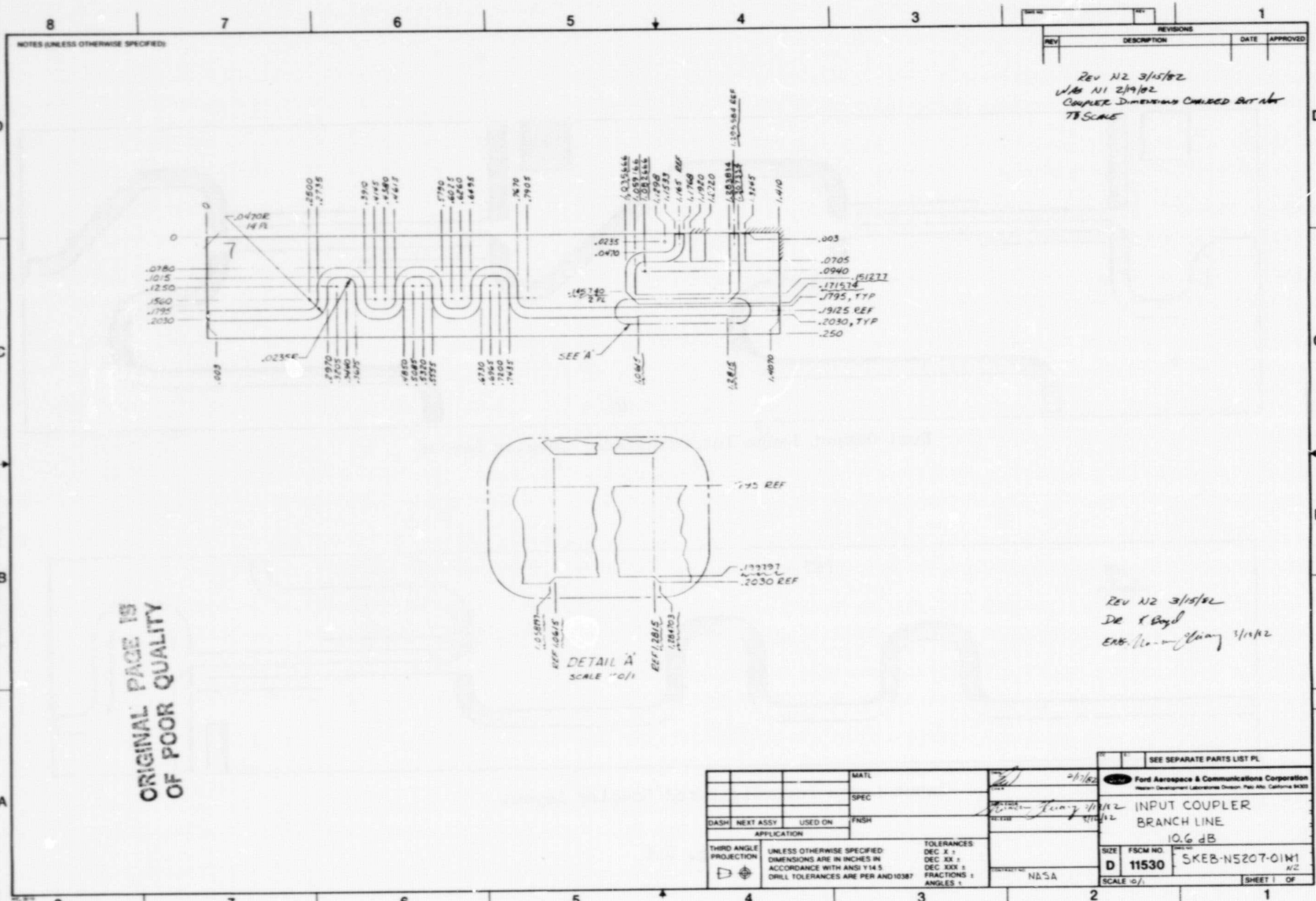
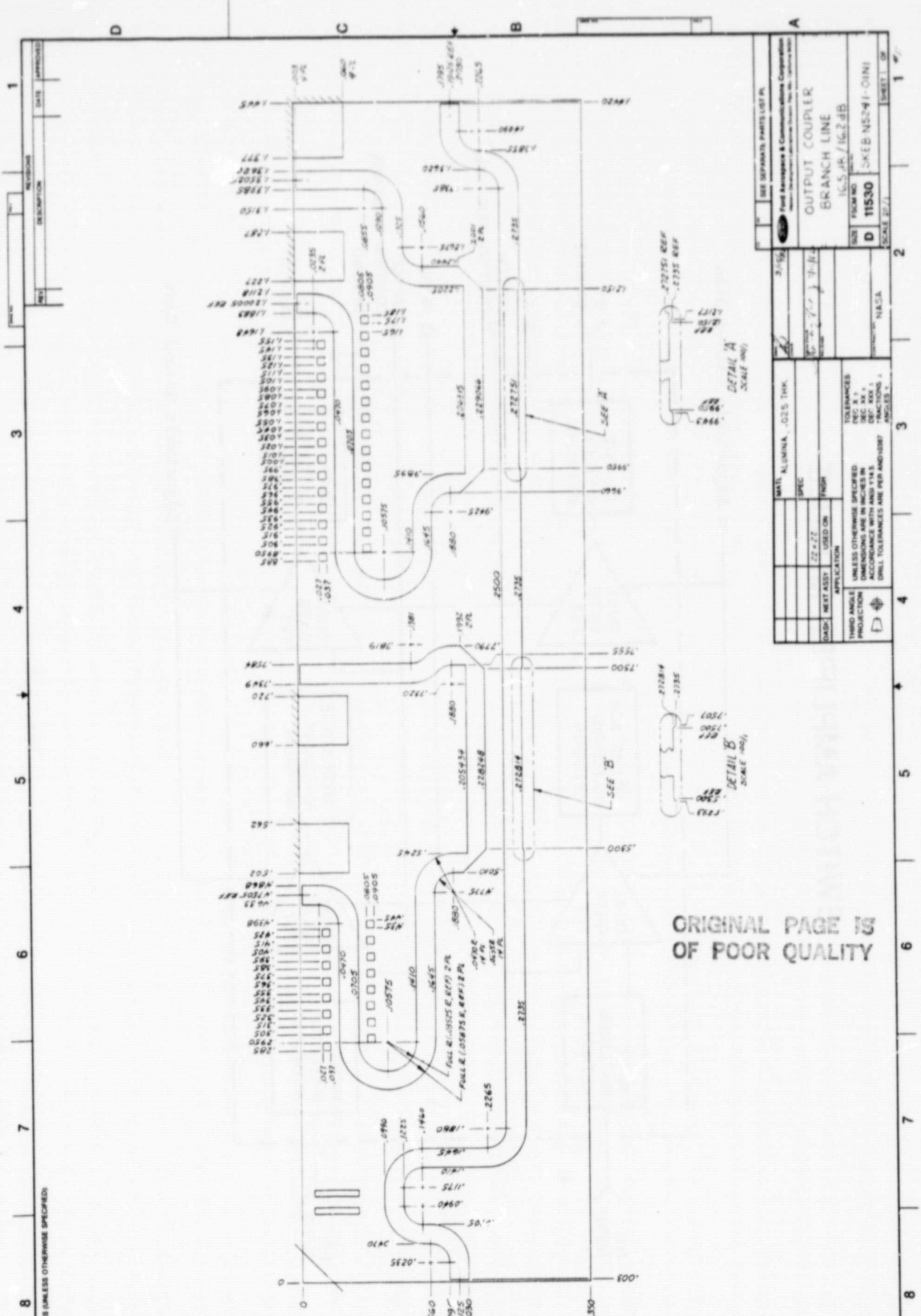

NOTES (UNLESS OTHERWISE SPECIFIED)
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
Rev N2 3/15/82
N1 2/19/82
COUPLER DIMENSIONS CHANGED BUT NOT TO SCALE
SEE 'A'
DETAIL 'A'
.745 REF
.2030 REF
Rev N2 3/15/82
MATL
SPEC
FNSH
DASH
NEXT ASSY
USED ON
APPLICATION
THIRD ANGLE PROJECTION
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES IN ACCORDANCE WITH ANSI Y14.5 DRILL TOLERANCES ARE PER AND10387
TOLERANCES
DEC X ±
DEC XX ±
DEC XXX ±
FRACTIONS ±
ANGLES ±
NASA
SEE SEPARATE PARTS LIST PL
Ford Aerospace & Communications Corporation
Western Development Laboratories Division, Palo Alto, California 94303
INPUT COUPLER
BRANCH LINE
10.6 dB
SIZE
FSCM NO.
D
11530
SKEB-N5207-01M1
N2
SHEET 1 OF

Fig. 2.7



Ford Aerospace & Communications Corporation
OUTPUT COUPLER
BRANCH LINE
16.5 dB / 16.2 dB
D
11530
SKEB N5241-01N1
ALUMINA, .025 THK.
NASA
DETAIL 'A'
DETAIL 'B'
SEE 'A'
SEE 'B'
THIRD ANGLE PROJECTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES IN ACCORDANCE WITH ANSI Y14.5
NOTES (UNLESS OTHERWISE SPECIFIED)

Fig. 2.8

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SWITCH AMPLIFIER MODULE

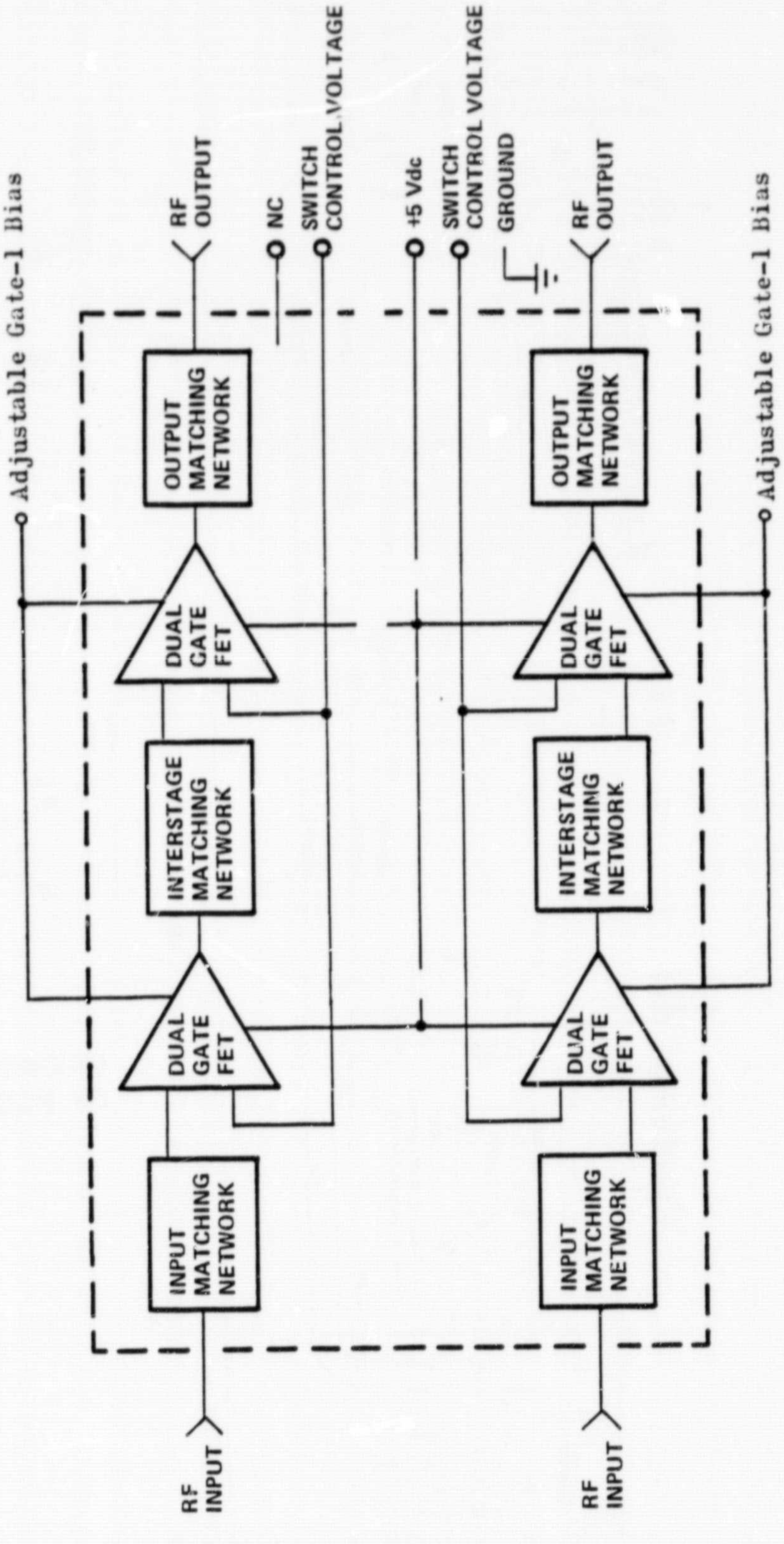


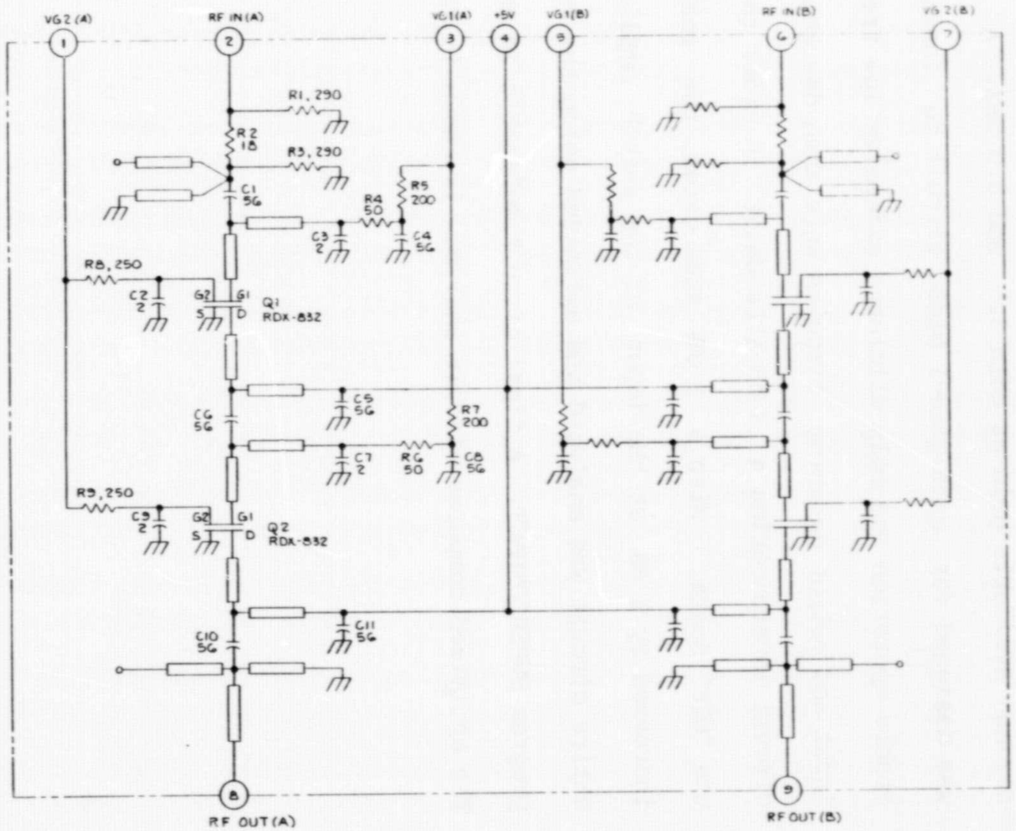
Fig. 3.1

1-dB Compression Point	@ Input = -20 dBm minimum
Maximum Input Power	0 dBm (CW, Survival)
Switching Speed (rise or fall)	10 nsec maximum
Phase Linearity Variation	$\pm$ 5 degrees

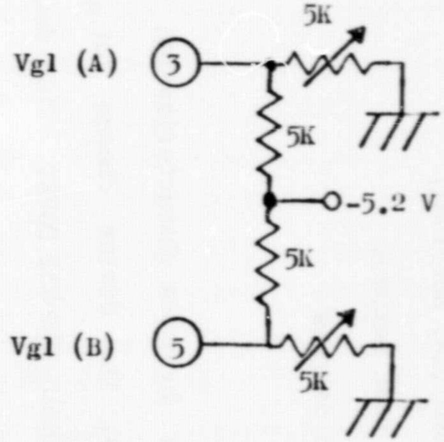
3.2 Design Approach - Electrical

The electrical design began with the in-house characterization and evaluation of several dual-gate FETs. The device chosen for the microwave switch amplifier is the Raytheon RDX-832 DGFET. This device provides good electrical performance while providing ease of handling and assembly. From the measured S-parameter, the interstage matching circuit was designed to have a flat frequency response optimized for maximum available gain at both 3.5 and 6.0 GHz. A stability circuit was designed for each gate-1 bias circuit to insure unconditionally stable operation and help eliminate excessive low frequency gain. The input and output matching circuits were then designed with the input circuit incorporating a 3 dB attenuator in order to improve VSWR in the "OFF" state. With a 3 dB attenuator, the return loss will be increased by 6 dB at the input of the switch amplifier module. The entire circuit was analyzed and optimized using the microwave analysis program SUPERCOMPACT. A final circuit schematic is shown in Fig. 3.2. The optimized computer circuit analysis is shown in Table 3.1.

SWITCH AMPLIFIER MODULE



External Bias Circuit



CIRCUIT IS MIRROR IMAGE & VALUES ARE THE SAME
RESISTORS ARE IN OHMS
CAPACITORS ARE IN PF.

Fig. 3.2

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Table 3.1

MICROWAVE SWITCH AMPLIFIER CIRCUIT SUPERCOMPACT ANALYSIS

FREQ	S11		S21		S12		S22		|S21|	STAB
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	db	K
3.00	0.187	-67	6.839	-40	0.001	-138	0.895	112	16.70	27.2
3.10	0.177	-98	8.463	-80	0.001	-178	0.845	107	18.55	24.6
3.20	0.185	-118	8.603	-117	0.001	143	0.801	101	18.69	27.5
3.30	0.210	-136	8.071	-146	0.001	114	0.764	94	18.14	32.7
3.40	0.237	-154	7.611	-170	0.001	92	0.726	86	17.63	39.7
3.50	0.265	-171	7.429	169	0.001	75	0.686	76	17.42	49.0
3.60	0.288	175	7.381	150	0.001	58	0.638	65	17.36	57.3
3.70	0.304	163	7.333	132	0.001	39	0.578	51	17.31	59.7
3.80	0.312	153	7.240	114	0.001	20	0.514	34	17.19	60.2
3.90	0.313	142	7.101	97	0.001	5	0.461	15	17.03	64.3
4.00	0.310	132	7.011	81	0.001	-9	0.423	-6	16.92	70.2
4.10	0.309	121	7.045	63	0.001	-24	0.403	-30	16.96	74.6
4.20	0.307	111	7.128	46	0.001	-40	0.405	-55	17.06	76.4
4.30	0.302	99	7.179	29	0.001	-56	0.428	-78	17.12	75.3
4.40	0.292	86	7.195	13	0.001	-71	0.463	-98	17.14	70.6
4.50	0.280	71	7.198	-3	0.001	-84	0.501	-113	17.14	63.5
4.60	0.266	56	7.243	-19	0.001	-93	0.533	-124	17.20	58.3
4.70	0.254	40	7.366	-35	0.001	-99	0.555	-134	17.34	57.1
4.80	0.243	21	7.494	-51	0.001	-107	0.569	-143	17.49	56.8
4.90	0.239	0	7.554	-66	0.001	-122	0.578	-151	17.56	53.4
5.00	0.244	-25	7.630	-82	0.001	-140	0.587	-159	17.65	47.5
5.10	0.259	-48	7.824	-100	0.001	-157	0.598	-167	17.87	41.1
5.20	0.280	-70	8.040	-119	0.001	-173	0.601	-176	18.11	37.8
5.30	0.304	-88	8.143	-136	0.001	171	0.587	176	18.22	39.8
5.40	0.326	-104	8.099	-152	0.001	156	0.562	168	18.17	45.0
5.50	0.347	-118	7.944	-169	0.001	142	0.537	161	18.00	49.7
5.60	0.366	-131	7.879	173	0.001	127	0.511	153	17.93	53.0
5.70	0.380	-142	8.055	154	0.001	111	0.478	141	18.12	55.4
5.80	0.394	-153	8.259	133	0.001	95	0.433	127	18.34	57.8
5.90	0.406	-162	8.181	112	0.001	82	0.375	110	18.26	61.8
6.00	0.415	-170	7.810	90	0.001	70	0.312	89	17.85	69.3
6.10	0.421	-177	7.296	69	0.001	57	0.263	62	17.26	80.6
6.20	0.425	177	6.677	47	0.001	41	0.247	29	16.49	95.2
6.30	0.427	171	5.920	26	0.001	23	0.277	-3	15.45	113.8
6.40	0.430	166	5.099	6	0.001	4	0.335	-28	14.15	138.4
6.50	0.432	161	4.333	-12	0.000	-12	0.403	-46	12.74	169.2

3.3 Switch Module Package Design

The major emphasis in the switch module package design was to develop a small light weight unit that will require minimal assembly time and can be easily aligned and tested. A module package was chosen incorporating two microwave switch crosspoints per module and using 50 ohm glass to metal feedthroughs for the RF interconnecting. The MIC housing outline is presented in Fig. 3.3. Both microwave switch circuits are mounted on a single 0.010" x 0.660" x 1.060" Alumina (Aluminum oxide) substrate with excellent electrical and physical properties. A chip DGFET device was chosen to reduce the total size and weight of the package. All component ground paths are provided by .020" diameter gold plated via holes through the substrate. All attenuator and bias resistors are thin film tantalum nitrite that are etched directly on the alumina substrate. Each module has the capability to be hermetically sealed by the application of beam welded cover. Module alignment and testing is accomplished by installing each module into a specially designed test fixture that simultaneously interconnects all DC and RF lines. (See Fig. 3.4) The adjustable Gate-1 voltage for each crosspoint is provided by a dual thick film bias circuit attached on top of the module cover. A brief summary of the switch module mechanical specifications are shown below.

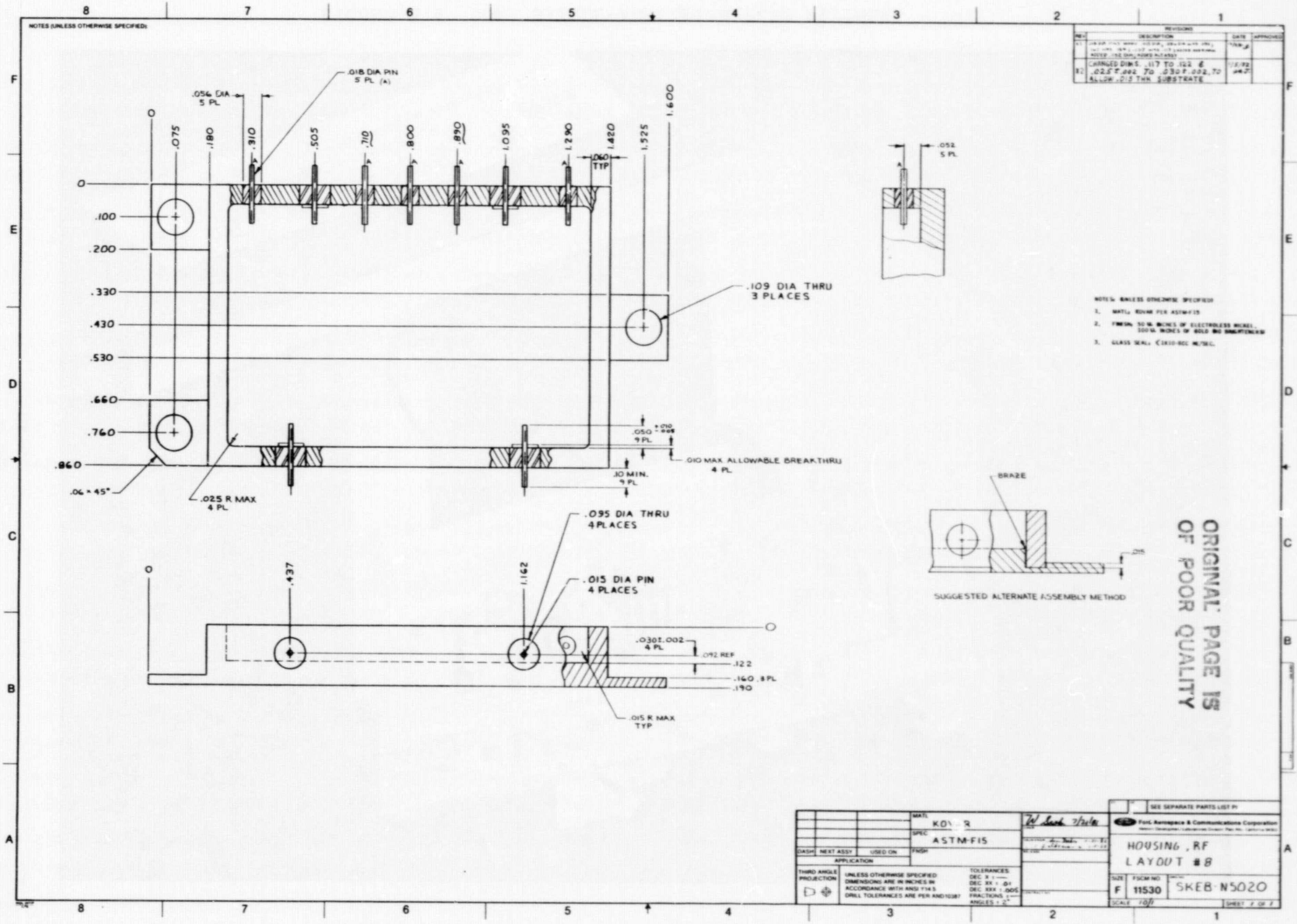

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Fig. 3.3

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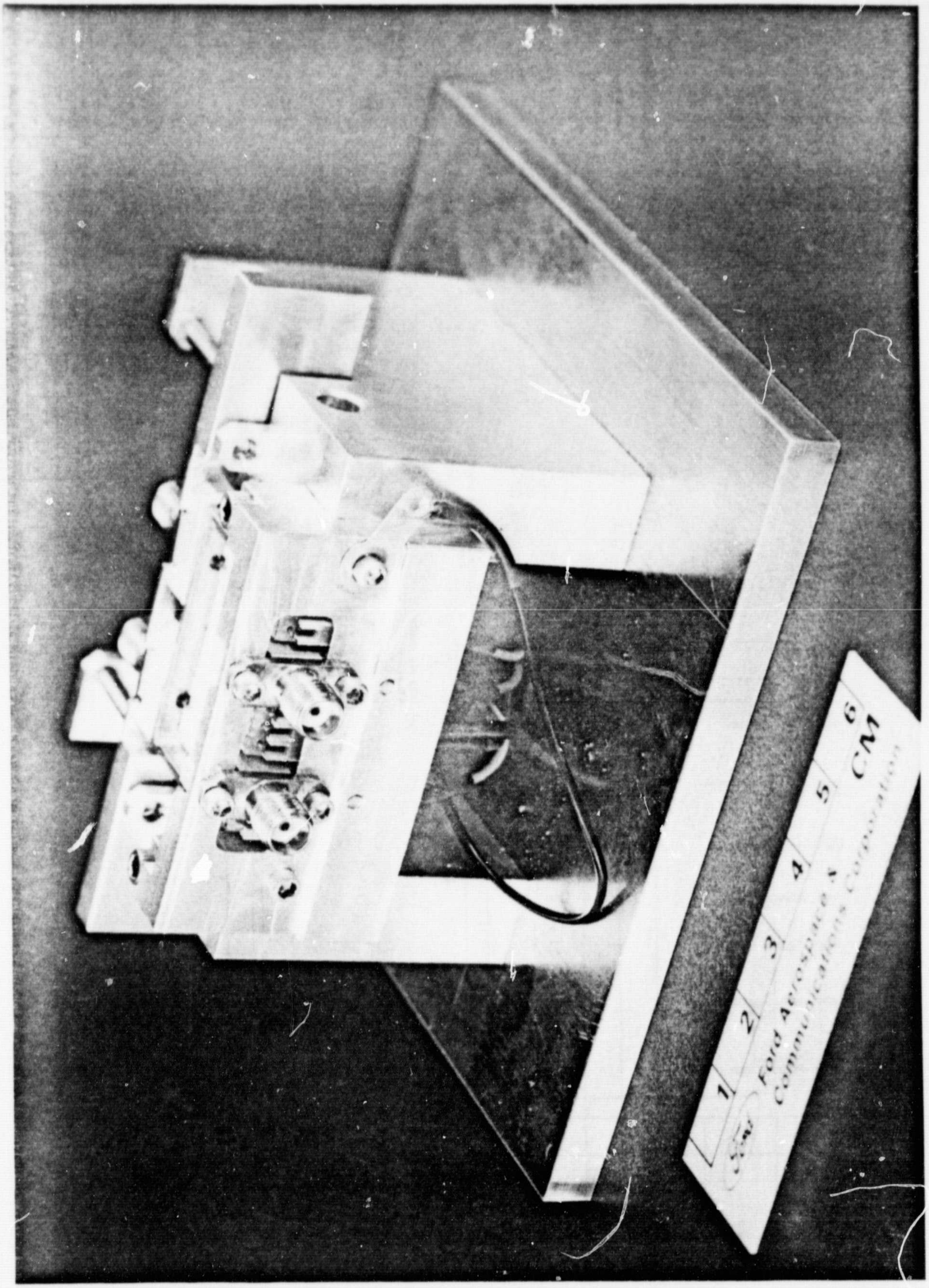

FIGURE 3.4 DUAL SWITCH-AMPLIFIER TEST FIXTURE

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MECHANICAL SPECIFICATIONS

Module Size	0.185" x 0.860" x 1.240"
Substrate Size	0.010" x .660" x 1.060"
Number of RF Feedthroughs	4
Number of Bias Feedthroughs	5
Module Weight	16.7 grams
Bias Substrate Size	.025" x .065" x .74"

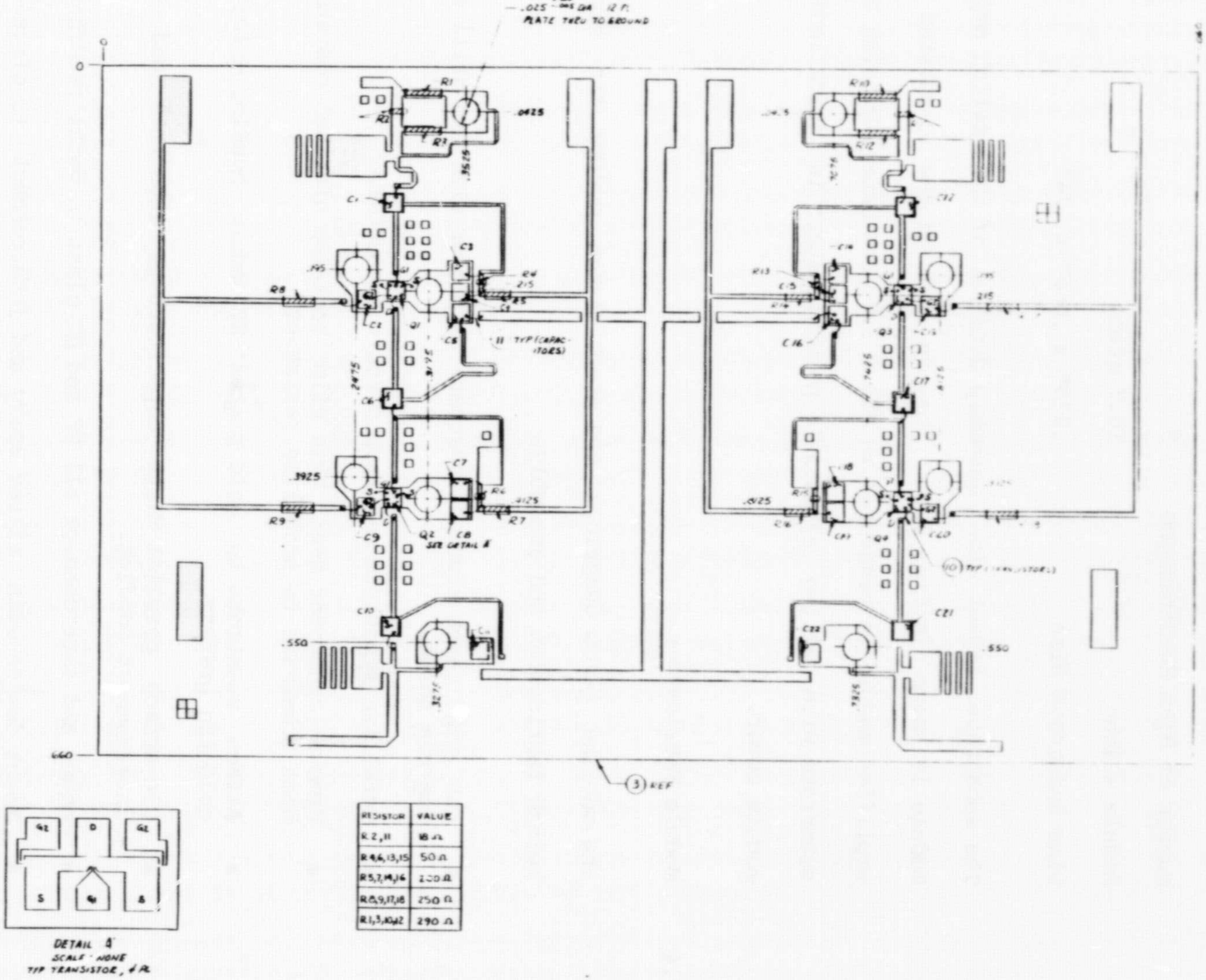
The substrate layout with assembly details of the switch amplifier module is shown in Fig. 3.5. The top view of the completed switch amplifier module is presented in Fig. 3.6 The Gate-1 biasing circuit substrate with the two adjustable potentiometers is installed on the module cover.

3.4 Module Fabrication

The outline below describes the steps taken during the microwave switch fabrication and assembly.

- Cut .010" thick alumina substrate to proper size and drill grounding via holes.
- Metallize substrate and etch circuit conductor.
- Remove conductor over thin film tantalum nitrite resistors and heat substrate to stabilize resistors.
- Attach substrate to gold plated RF module housing using 80/20 gold-tin preform.
- Die-attach parallel plate capacitors to substrate and do all interconnect bonding.
- Mount and interconnect all RF and DC glass to metal feedthrus.
- Mount device with silver epoxy and interconnect to circuit using .0007" gold wire.
- Place device in test fixture for individual module alignment and testing.

SWITCH AMPLIFIER MODULE LAYOUT



RESISTOR	VALUE
R 2, 11	18 Ω
R 4,6,13,15	50 Ω
R 5,7,14,16	200 Ω
R 8,9,17,18	250 Ω
R 1,3,10,12	290 Ω

Fig. 3.5

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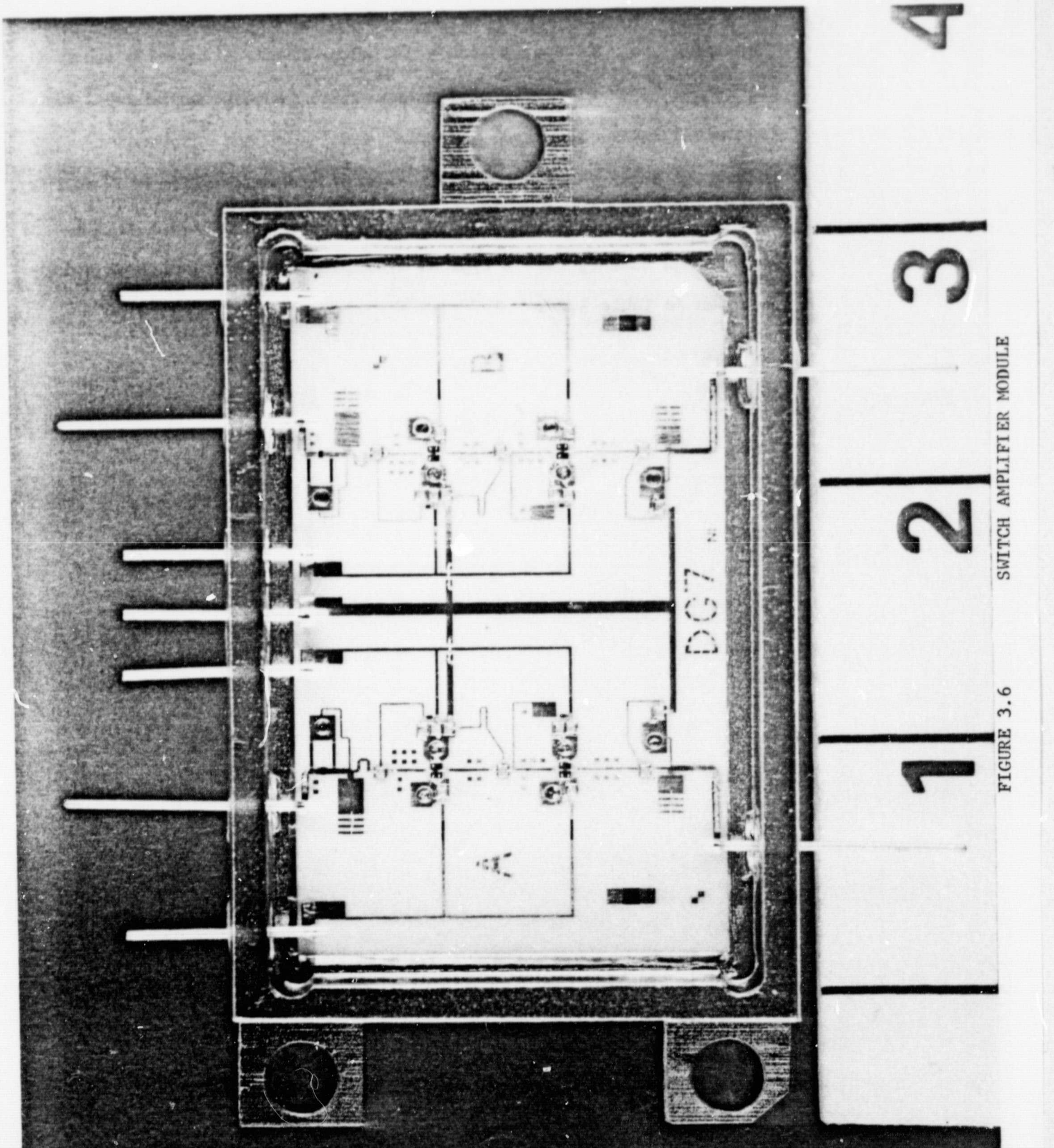

FIGURE 3.6 SWITCH AMPLIFIER MODULE

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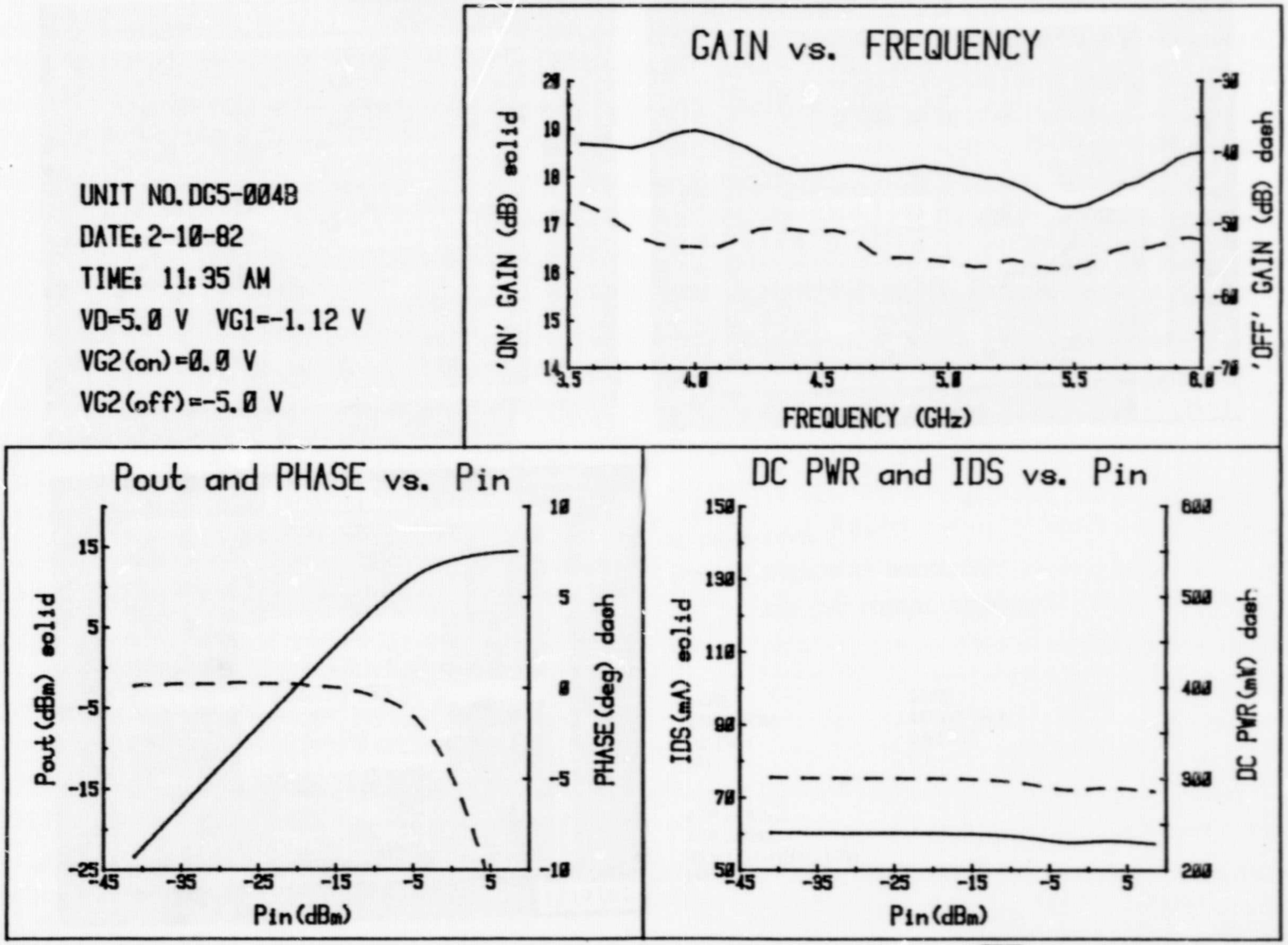
3.5 Experimental Test Results

Each individual crosspoint module is independently tested and tuned on the bench. The microwave switch amplifier performs quite well with little alignment required. Sample data for one crosspoint (1/2 module) is shown in Figure 3.7. Switching speed performance of the switch amplifier plus the switch driver is presented in Fig. 3.8. A performance summary for a typical crosspoint switch amplifier module is shown in Table 3.2 .

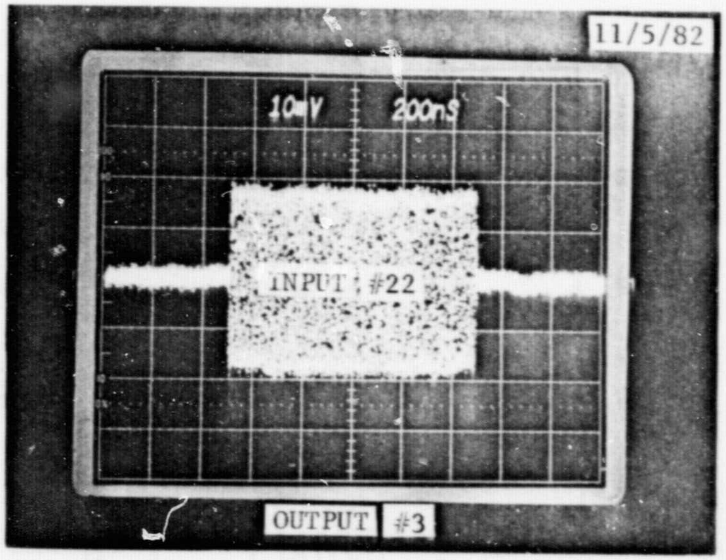
SWITCH/AMPLIFIER TEST DATA

UNIT NO. DG5-004B
DATE: 2-10-82
TIME: 11:35 AM
VD=5.0 V VG1=-1.12 V
VG2(on)=0.0 V
VG2(off)=-5.0 V



Ford Aerospace & Communications Corporation

Fig. 3.7

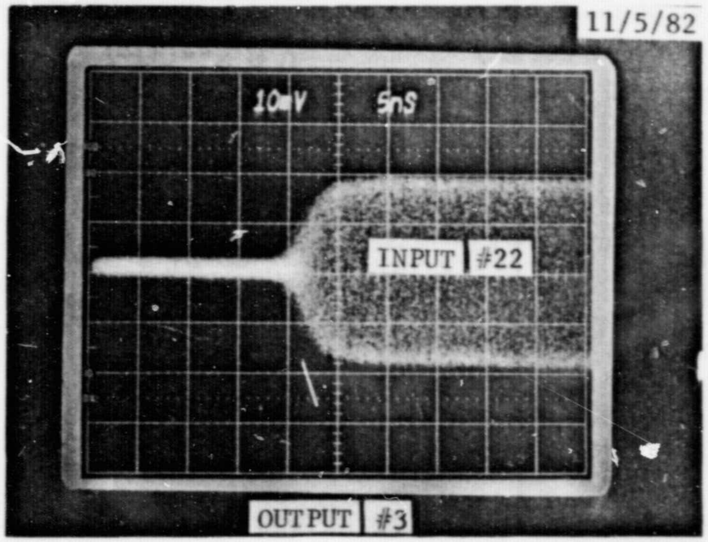


(a)
STATE DURATION
1 μs "ON"
4 μs "OFF"

(b)
DETAIL
TURN-ON
TIME

(c)
DETAIL
TURN-OFF
TIME

TYPICAL OUTPUT SIGNAL
SHOWING SWITCHING DURATIONS
OF LESS THAN 5 ns



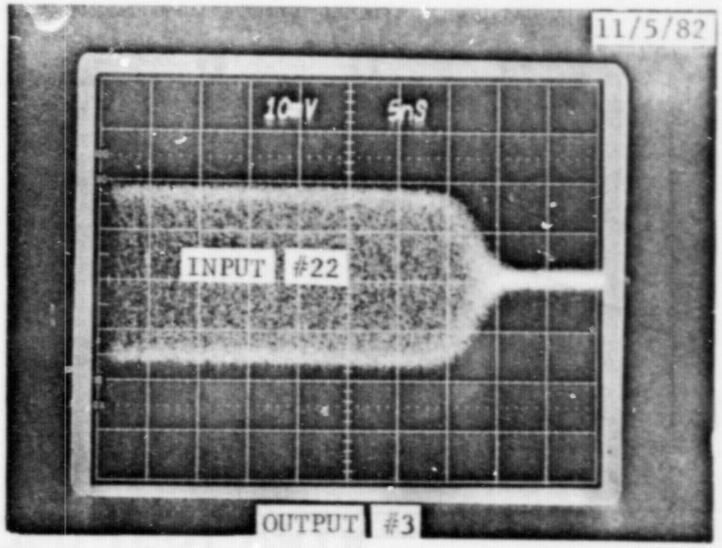


Fig. 3.8

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TABLE 3.2

SWITCH AMPLIFIER PERFORMANCE CHARACTERISTICS

Parameter	Goal	Performance
Frequency Band	3.5 GHz to 6.0 GHz	3.5 GHz to 6.0 GHz
Bandwidth	1000 MHz	2500 MHz
Bandpass Ripple	$\pm$ 1.5 dB	$\pm$ 0.75 dB "ON" Gain
"ON" Gain	15.5 dB	18.0 dB
"ON" to "OFF" Isolation	53 dB	64 dB
1-dB Comp. Point	@ Pin = -20 dBm	@ Pin = -6 dBm
Switching Speed Rise Time	10 nsec	2.5 nsec
Fall Time	10 nsec	6 nsec
Maximum RF Input Power	0 dBm (CW, Survival)	10 dB (CW, Survival)
DC Pwr ("ON")	—	300 mW
DC Pwr ("OFF")	—	20 nW

3.6 Parts List

The main parts used for one of the 38 switch amplifier modules including the biasing substrate assembly are presented in the following table:

Item	Mfg: Part Number	Quantity
Dual-Gate FET	Raytheon RDX-832	4
Parallel Plate Capacitor 56 pF	ATC 111 SG 560 M 100 AP	14
Parallel Plate Capacitor 2 pF	ATC 111 S DB 2 RO C 100 AP	8
50 Ohm RF Feedthrus	Tekwave 10-1537-0000	4
DC Feedthrus	EI 7AS-17W-SS-MOD-L	5
RF Module Housing	Ford Dwg # N5033	1
RF Module Cover	Ford Dwg # N5035	1
5 K Ohm Mini-Potent.	Vishay 1240 P 5000 5%	2
RF Switch Amplifier Substrate	Ford Dwg #N5414-D1	1
External Bias Current Substrate	Ford Dwg # N5417	1

4.0 SWITCH-DRIVER MODULE

The switch-driver circuit is the interface circuit between the Dual-Gate GaAs FET switch-amplifier and the distribution control unit.

The switch-driver circuit provides the necessary voltages to the second gate of the dual gate GaAs FET (switch amplifier module) to achieve The "ON" and "OFF states. When the Gate-2 control voltage is zero or slightly positive, the two-stage switch-amplifier is "ON". When the control voltage is sufficiently negative (-5.2 volts), the switch-amplifier is "OFF", and high isolation between input and output parts is achieved for the corresponding signal path.

The switching time of the IF switch matrix is determined principally by the switch-driver circuit since the switching time of the Dual-Gate GaAs FET is extremely fast (0.1 nanoseconds). The capability of the switch-driver circuit to deliver fast turn on and turn off voltages to the second gate of the Dual-Gate GaAs FET depends on the response of the switch driver transistor and on the total capacitance in parallel with the driver transistor output.

The requirements of the switch-driver are summarized as follows:

1. Fast "ON-OFF" Switching Time. The switching time is mainly dependent on the cutoff frequency of the switching transistor, the necessary Gate-2 voltage, and the parasitic capacitance of the circuit associated with the control of the second gate, including the interconnection circuit between modules. The interconnection between the switch driver module output and the switch amplifier module is made by a printed circuit board and glass feedthrus. A shorter switching time could be obtained if both the switch

amplifier and switch driver were fabricated on the same substrate using thin film technology.

2. Low Power Consumption in the "ON" State. The power consumption for the "ON" state is very important because of the 20 "ON" switches which can occur in a 20 x 20 switch matrix.

3. Very Low or preferably no Power Consumption in the "OFF" State. For a switch matrix N(N-1) of the switches is in "OFF state. For a 20 x 20 matrix, the number of switches in the "OFF" state, at any time is 380. The block diagram of the switch-driver module is presented in Fig. 4.1. One module is associated with each set of two adjacent crosspoints of the matrix. Each module contains a dual switch-driver stage using high-speed bipolar transistors controlled through an integrated dual flip-flop integrated circuit. The switching is controlled by the signal from the decoder logic of the distribution control unit and triggered by the data transfer signal, also supplied by the DCU.

The schematic of the switch-driver circuit is presented in Fig. 4.2. It is a single transistor switch-driver circuit controlled by a flip-flop circuit, the 54LS74 integrated circuit. The data transfer pulse from the DCU determines the moment when the configuration of the IF switch matrix is initiated. This data transfer pulse is distributed to each driver circuit board by the data transfer circuit (see schematic Fig. 4.3). The PC board lay-out for this circuit is shown in Fig. 4.4. The operation of the switch driver is as follows. If the voltage at the input of the flip-flop supplied by the DCU, is zero, the switch driver circuit output voltage is +0.2 V and the corresponding crosspoint is

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SWITCH DRIVER MODULE

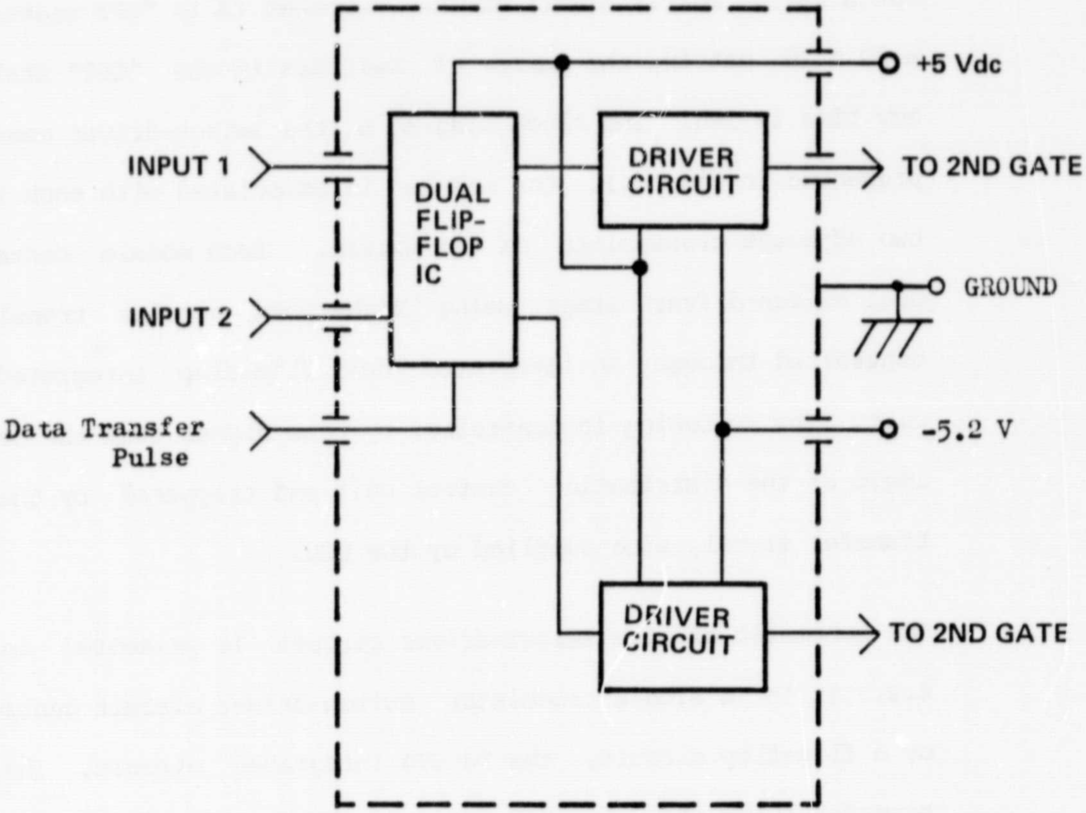
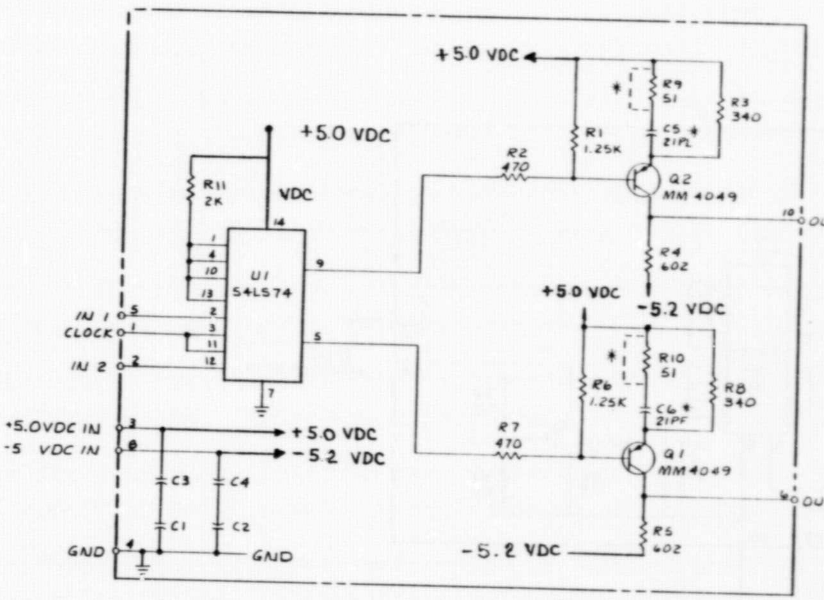


Fig. 4.1

SWITCH DRIVER MODULE



NOTE:
I-6 VERSION SHOWN; FOR NASN VERSION
REPLACE R9 & R10 WITH JUMPER AND
C5 & C6 VALUES TO BE 10pF

Fig. 4.2 Switch Driver Module Schematic

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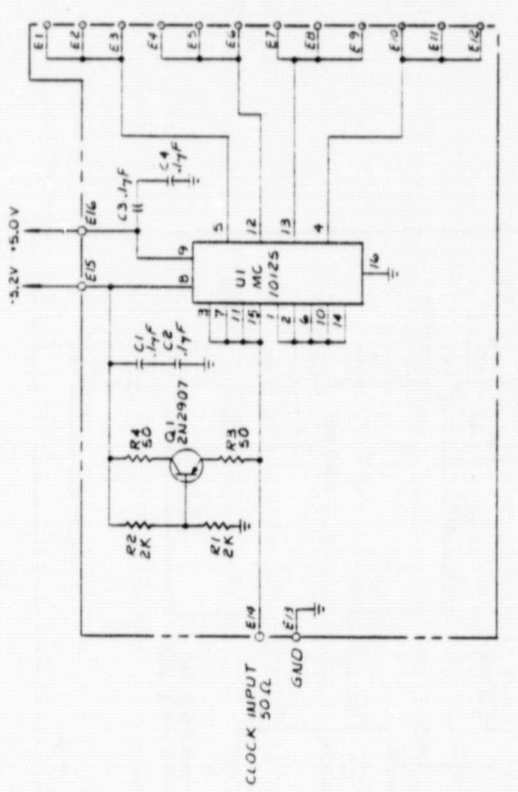

DATA TRANSFER CIRCUIT
Fig. 4.3

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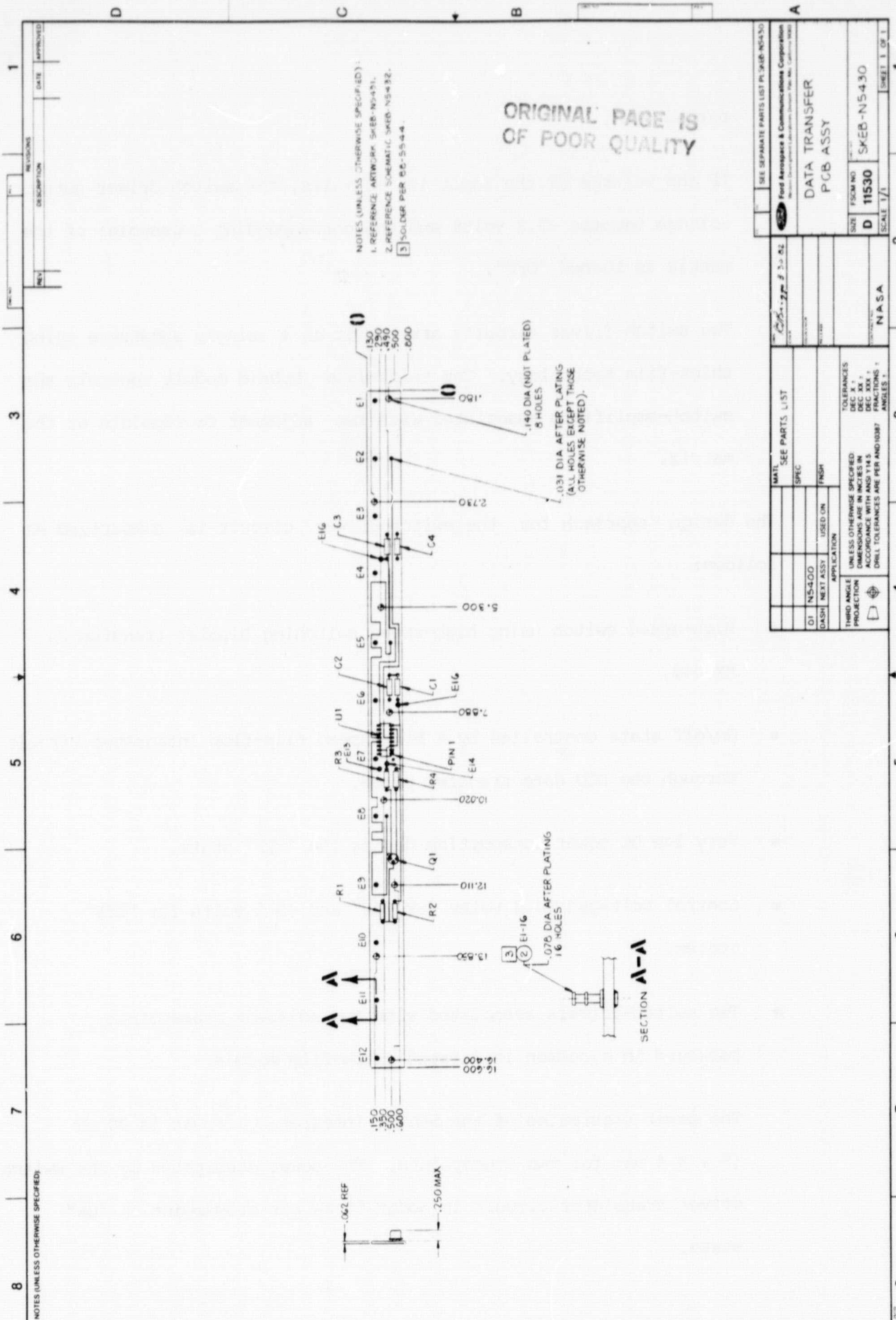

Fig. 4.4

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turned "ON".

If the voltage at the input is +5 volts, the switch driver output voltage becomes -5.2 volts and the corresponding crosspoint of the matrix is turned "OFF".

Two switch-driver circuits are built on a single substrate using thick-film technology. The thick-film hybrid module controls the switch-amplifiers associated with two adjacent crosspoints of the matrix.

The design approach for the switch-driver circuit is summarized as follows:

- High-speed switch using high-speed switching bipolar transistors MM4049.
- On/off state controlled by a high-speed flip-flop integrated circuit through the DCU data transfer pulse.
- Very low DC power consumption during the "OFF" state.
- Control voltages +0.2 volts for "ON" and -5.2 volts for "OFF" states.
- Two switch-drivers associated with two adjacent crosspoints packaged in a common integrated thick-film module.

The power dissipated of the 54LS74 integrated circuit is 20 mW (5 V @ 4 mA) for two crosspoints. The power dissipated by the switch-driver transistor circuit is about 55 mW per crosspoint in "ON" state.

The power dissipated by the switch-driver in the "OFF" state is about 15 mW per crosspoint. Approximately 10 mW are dissipated in the dual flip-flop IC and about 5 mW in the biasing circuit of the bipolar switching transistor.

Since, at any time, 380 crosspoints of the matrix are "OFF", the total power consumption of the switch-drivers is 20 x 0.055 + 380 x 0.015 = 6.8 watts.

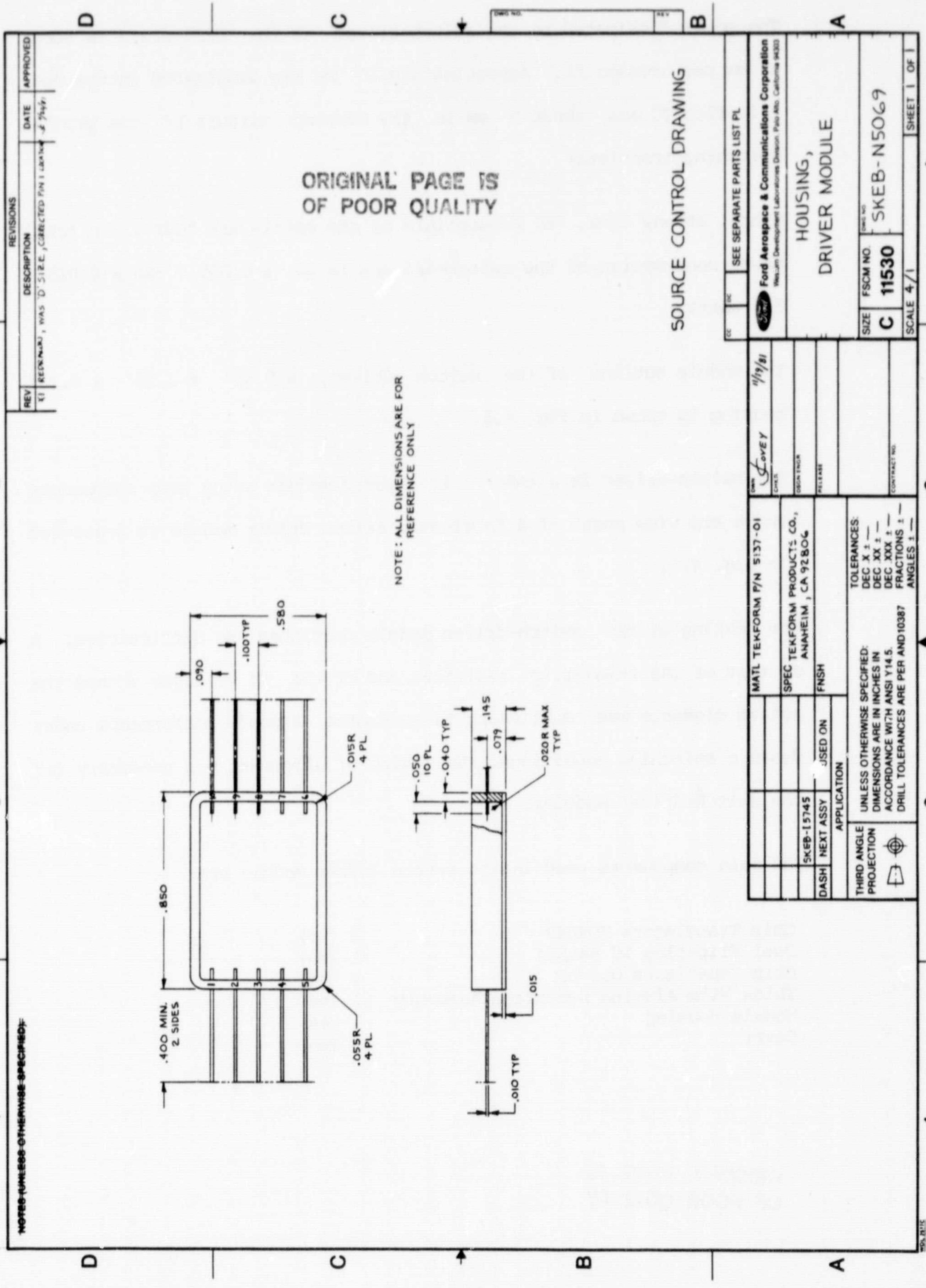
The module outline of the switch -driver, a 0.85" x 0.58" x 0.15" housing is shown in Fig. 4.5.

The switch-driver is a thick-film hybrid module using chip components and a top view photo of a fabricated switch driver module is presented in Fig. 4.6.

The testing of the switch-driver module presented no difficulties. A dc test of the thick-film resistors and of the dc voltages across the active elements was sufficient to guarantee a good performance under dynamic switching conditions. No tuning or alignment was necessary for the switch-driver modules.

The main components used in the switch driver module are:

Chip Transistors MM4049	2 (ea)
Dual Flip-flop IC 54LS74	1 (ea)
Chip Capacitors 0.1 uF	4 (ea)
Thick Film Alumina Substrate Assembly	1 (ea)
Module Housing	1 (ea)
Cover	1 (ea)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SOURCE CONTROL DRAWING
NOTE: ALL DIMENSIONS ARE FOR REFERENCE ONLY
REVISIONS
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SEE SEPARATE PARTS LIST PL
Ford Aerospace & Communications Corporation
HOUSING,
DRIVER MODULE
SIZE C
FSCM NO. 11530
SKEB-N5069
SCALE 4/1
SHEET 1 OF 1
MATL TEKFORM P/N 5137-01
SPEC TEKFORM PRODUCTS CO., ANAHEIM, CA 92806
FNSH
SKEB-15745
DASH NEXT ASSY USED ON
APPLICATION
THIRD ANGLE PROJECTION
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES IN ACCORDANCE WITH ANSI Y14.5. DRILL TOLERANCES ARE PER AND10387
TOLERANCES: DEC X ± — DEC XX ± — DEC XXX ± — FRACTIONS ± — ANGLES ± —
.850
.400 MIN. 2 SIDES
.055R 4 PL
.015R 4 PL
.090
.100 TYP
.580
.050 10 PL
.040 TYP
.145
.079
.020 R MAX TYP
.015
.010 TYP

Fig. 4.5

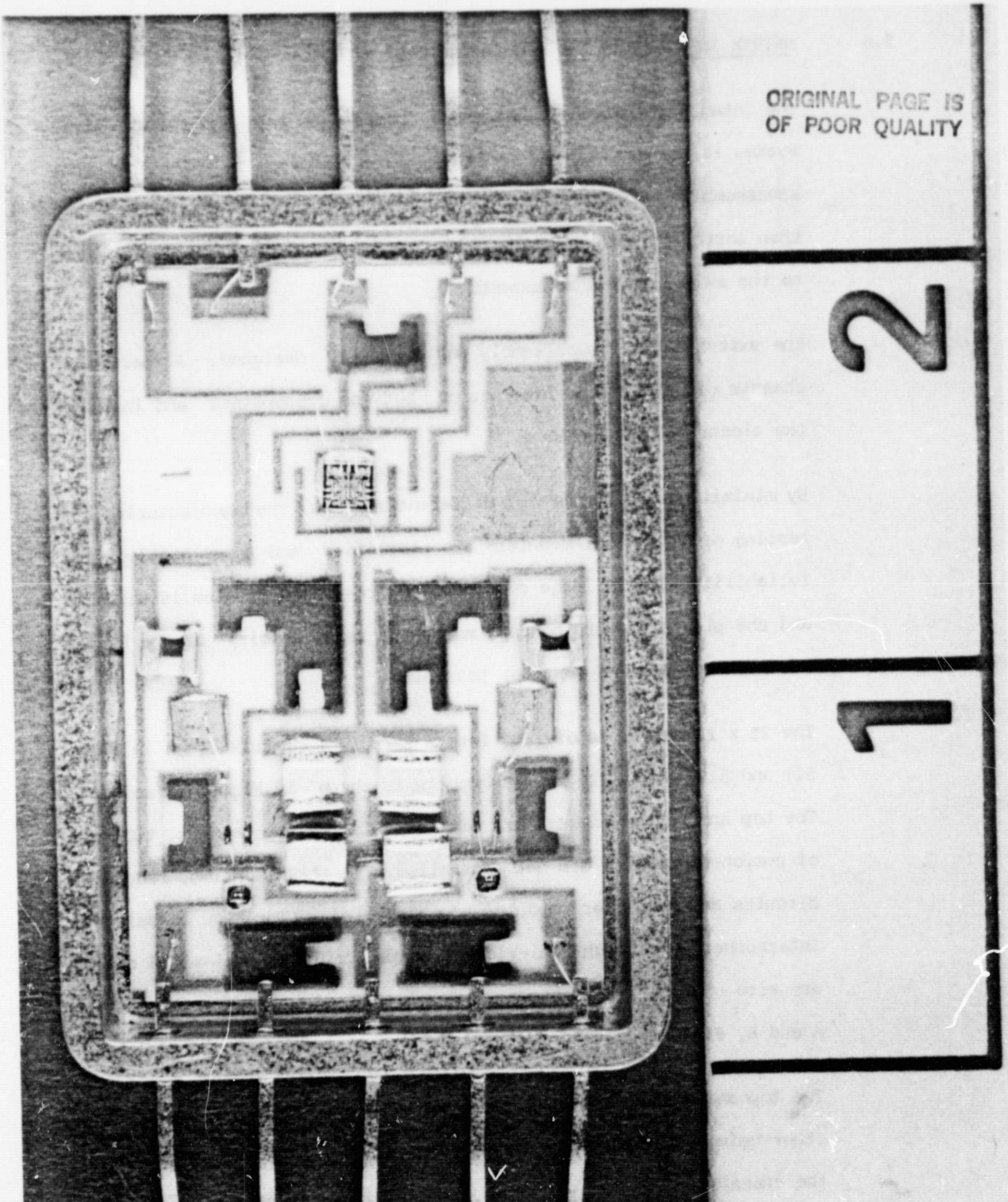

FIGURE 4.6 Dual Switch Driver Module

5.0 MATRIX INTEGRATION AND MECHANICAL DESIGN

The integration of the subassembly components into the switch matrix system is primarily based on the modular concept in which identical subassemblies or modules are individually assembled and tested, and then installed into a larger unit. The following description applies to the switch matrix subassembly.

The switch matrix subassembly was carefully designed. A partition chassis minimized the interaction between crosspoints and improved the electrical performance.

By minimizing the number of different modules the manufacturing and testing of identical modules are simplified and less costly. The reliability of this large system using pre-tested modules is enhanced and the planar layout concept makes the repairability of the system (during assembly and testing) possible.

The 22 x 22 matrix is divided into a 22 x 12 submatrix shown in Figs. 5.1 and 5.2, and a 22 x 10 submatrix is shown in Figs. 5.3 and 5.4. The top and bottom chassis are similar. In the top chassis, two rows of component modules are not installed. In this location, redundant circuits and amplifier modules are installed. The two chassis are interconnected through semi-rigid U-shaped cables. Semi-rigid cables are also used to interconnect the redundant signal paths (connectors A and B, Fig. 5.4).

The top and bottom chassis are folded over and mounted on top of each other using mounting bolts. Top and bottom covers are provided for the chassis.

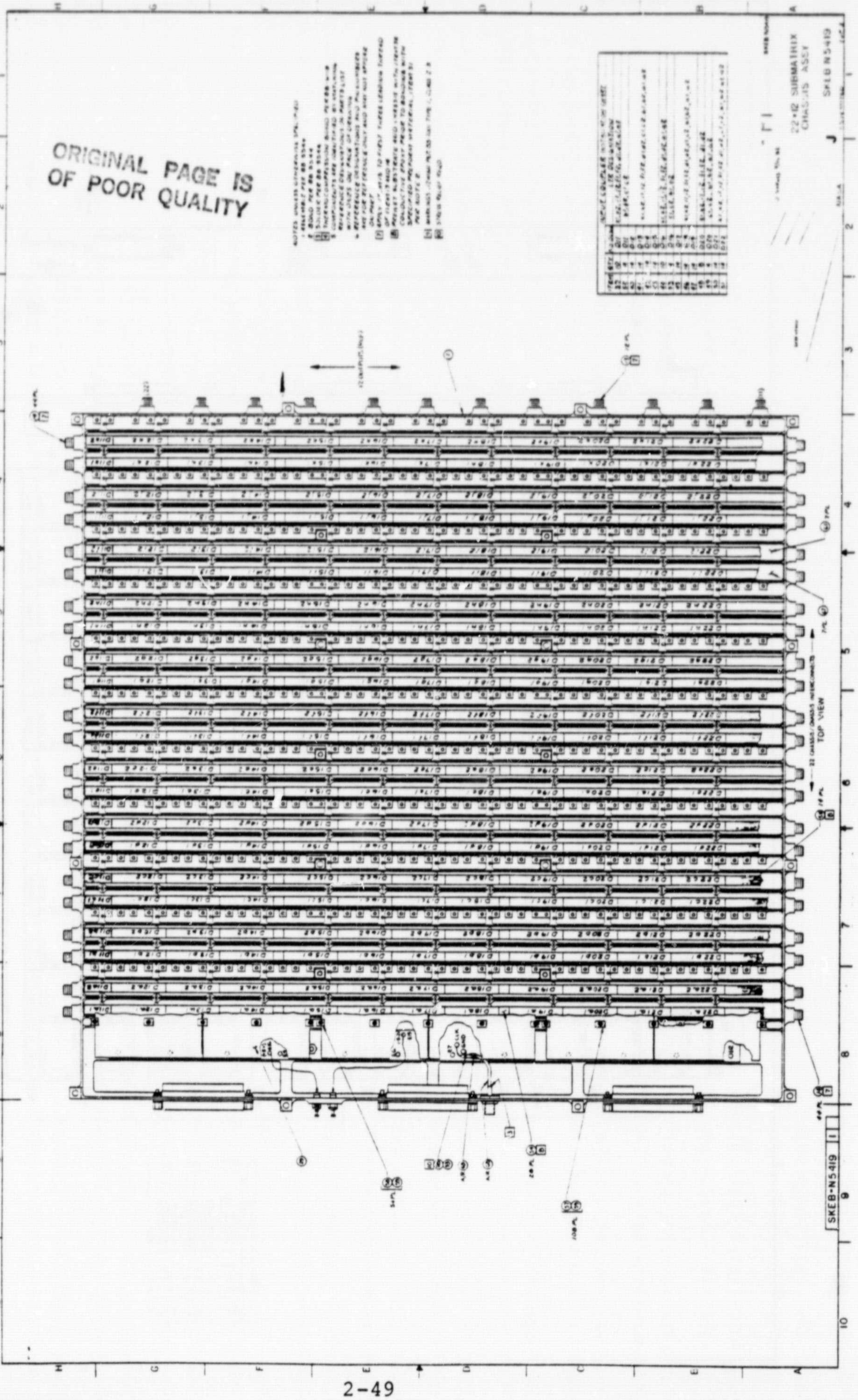

Fig. 5.1 Bottom Chassis

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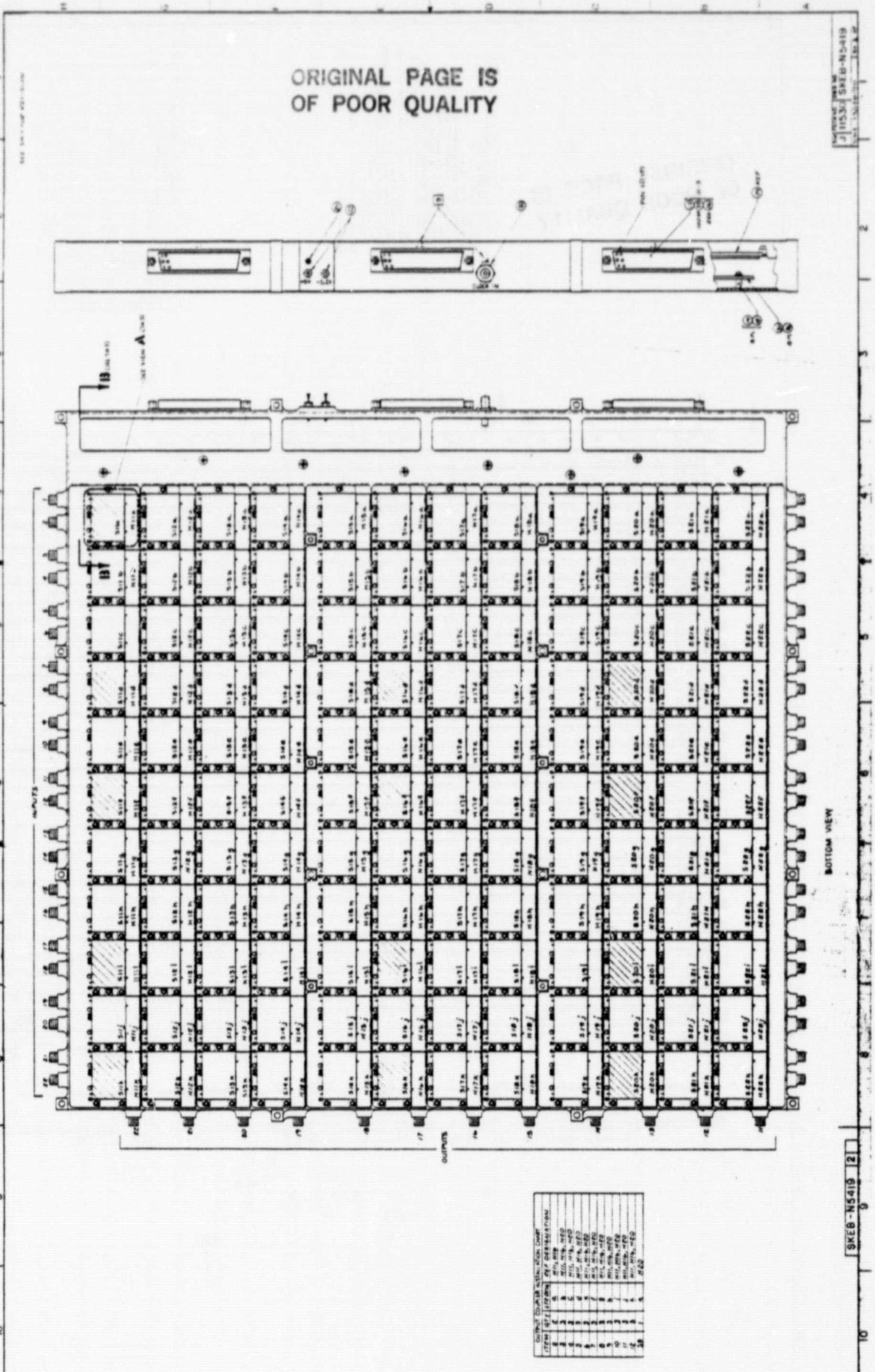

Fig. 5.2 Bottom Chassis

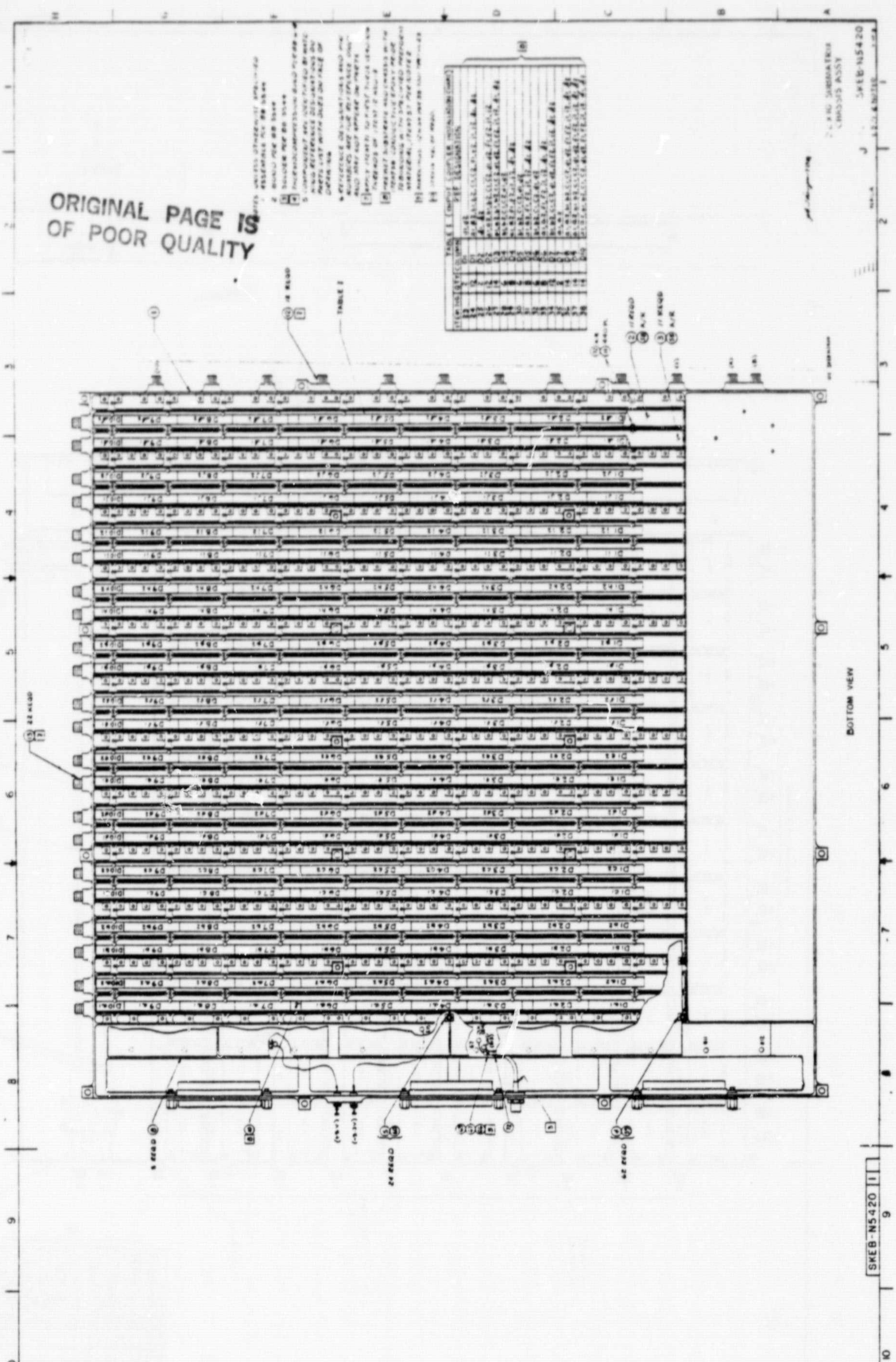

Fig. 5.3 Top Chassis

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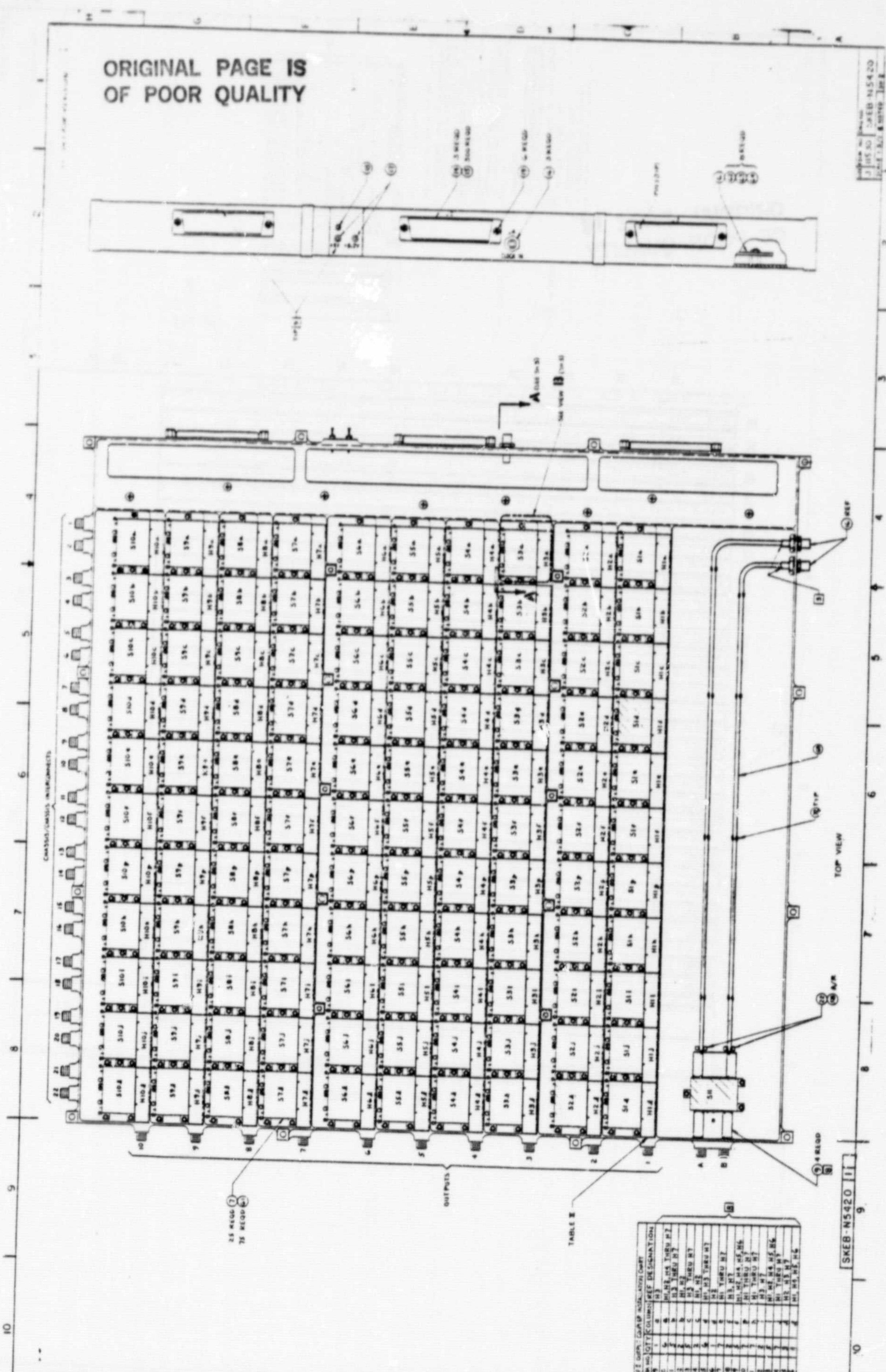

Fig. 5.4 Top Chassis

The top chassis (Fig. 5.3) includes 10 output connectors for columns 1 thru 8 of the switch matrix and 2 connectors for the redundant path interconnections. The bottom chassis includes 12 output connectors for columns 9 thru 20 of the switch matrix.

All 20 input connectors for the basic 20 x 20 matrix are installed on the bottom chassis. On the bottom chassis are also installed two connectors used in the redundant signal interconnection. Additional connectors, 22 on each chassis, are used for the RF signal when the two submatrices 22 x 12 and 22 x 10 are interconnected to become a 22 x 22 matrix.

The decoder logic signals from the DCU to each of 484 crosspoints of the matrix are supplied through a set of six 100 pin connectors (A, B, C, on the top chassis and D, E, F on the bottom chassis).

Each chassis is also supplied with the data transfer pulse (ECL voltage -0.8V to -1.85V) from the DCU, through 50 ohm coaxial cables and SMA connectors.

Each chassis is also supplied with the required DC input power through miniature RFI/EMI filters. For proper operation, the matrix needs +5.0 Vdc and -5.2 Vdc supply voltages.

Each chassis has two mounting surfaces. On one surface are installed the input couplers and the switch driver modules; on the opposite surface are installed the switch amplifier modules and the output couplers. Interconnection between the two surfaces of the chassis is by feedthrus supplying the RF and DC control voltages for the switch amplifier modules. For each module (e.g., for each pair of crosspoints of the matrix), there are 6 feedthrus, 2 for the RF input

signal, 2 for the corresponding Gate 2 control voltages from the switch-driver module output, one for +5 volts drain voltage and one for -5.2 volts DC Gate-1 Bias voltage.

The control and DC voltages are provided through the switch driver board assemblies. There are eleven multilayer PC boards (five in the top chassis and six in the bottom chassis). On these boards are soldered all switch-driver modules. Printed traces are used to distribute the DC voltages to each driver module on the board and then ultimately to each switch amplifier module on the other surface of the chassis. This same PC board also distributes the data transfer pulse to each of the switch driver module inputs.

The data signal from the six 100 pin connectors A, B, C,...through F is supplied to the switch driver modules using insulated flexible wires.

The RF signal from the coupled ports of the series connected input couplers is transmitted to the switch amplifier module through the 50 ohm RF feedthrus installed very close to each of the coupled ports of the input couplers. Details on this interfacing are presented in Fig. 5.5.

In each chassis, there is also installed a printed circuit board for the data transfer pulse. This data transfer circuit takes the ECL signal from the distribution control unit and converts it into 12 TTL signals. Each of these data transfer pulses is distributed, with equal propagation delay, to all the switch driver modules corresponding to the crosspoints on a column of the matrix.

The top and bottom view of the top chassis is presented in Figs. 5.3

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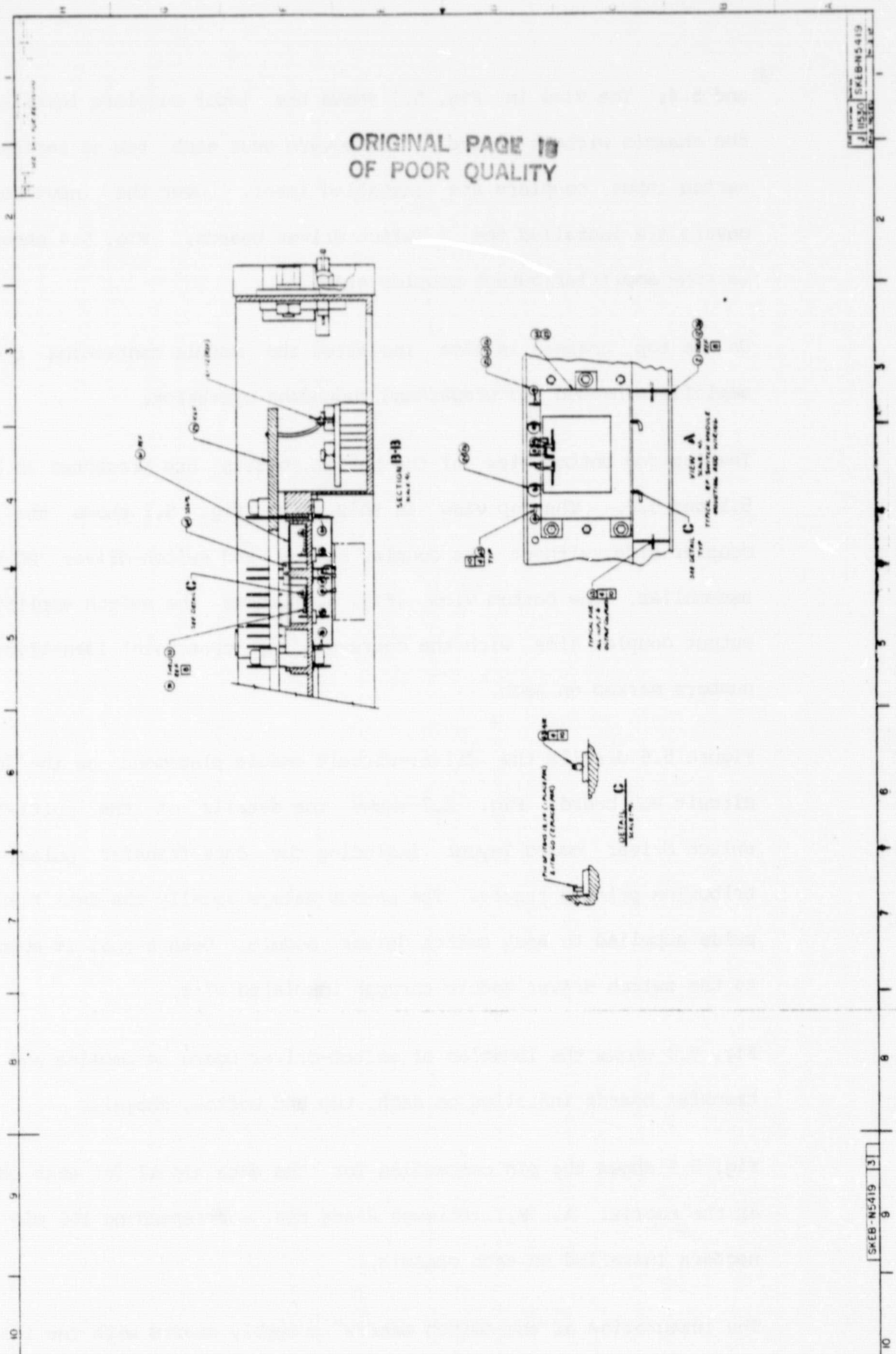

Fig. 5.5 RF Module Interfacing Diagram

and 5.4. The view in Fig. 5.3 shows the input couplers installed on the chassis without covers. The covers over each row of series connected input couplers are installed later. Over the input coupler covers are installed the 5 switch driver boards. Fig. 5.4 shows the switch- amplifier/output coupler side.

On the top chassis is also installed the module containing the two amplifiers needed for wraparound redundant operation.

The top and bottom view of the bottom chassis are presented in Figs. 5.1 and 5.2. The top view in this case (Fig. 5.1 shows the input coupler side, without the coupler covers and switch-driver PC board assemblies. The bottom view (Fig. 5.2) shows the switch amplifier/-output coupler side with the corresponding crosspoint identification numbers marked on each.

Figure 5.6 details the driver-circuit module placement on the driver circuit PC board. Fig. 5.7 shows the details of the multi-layer switch driver board layout including the data transfer pulse distribution printed traces. The layout delays equally the data transfer pulse supplied to each switch driver module. Data signal is supplied to the switch driver module through insulated wires.

Fig. 5.8 shows the location of switch-driver board assemblies and data transfer boards installed on each, top and bottom, chassis.

Fig. 5.9 shows the pin connection for the data signal for each column of the matrix. A, B,...through F are the corresponding 100 pin connectors installed on each chassis.

The integration of the switch matrix assembly starts with the installation of the feedthru using silver epoxy. Next step is the instal-

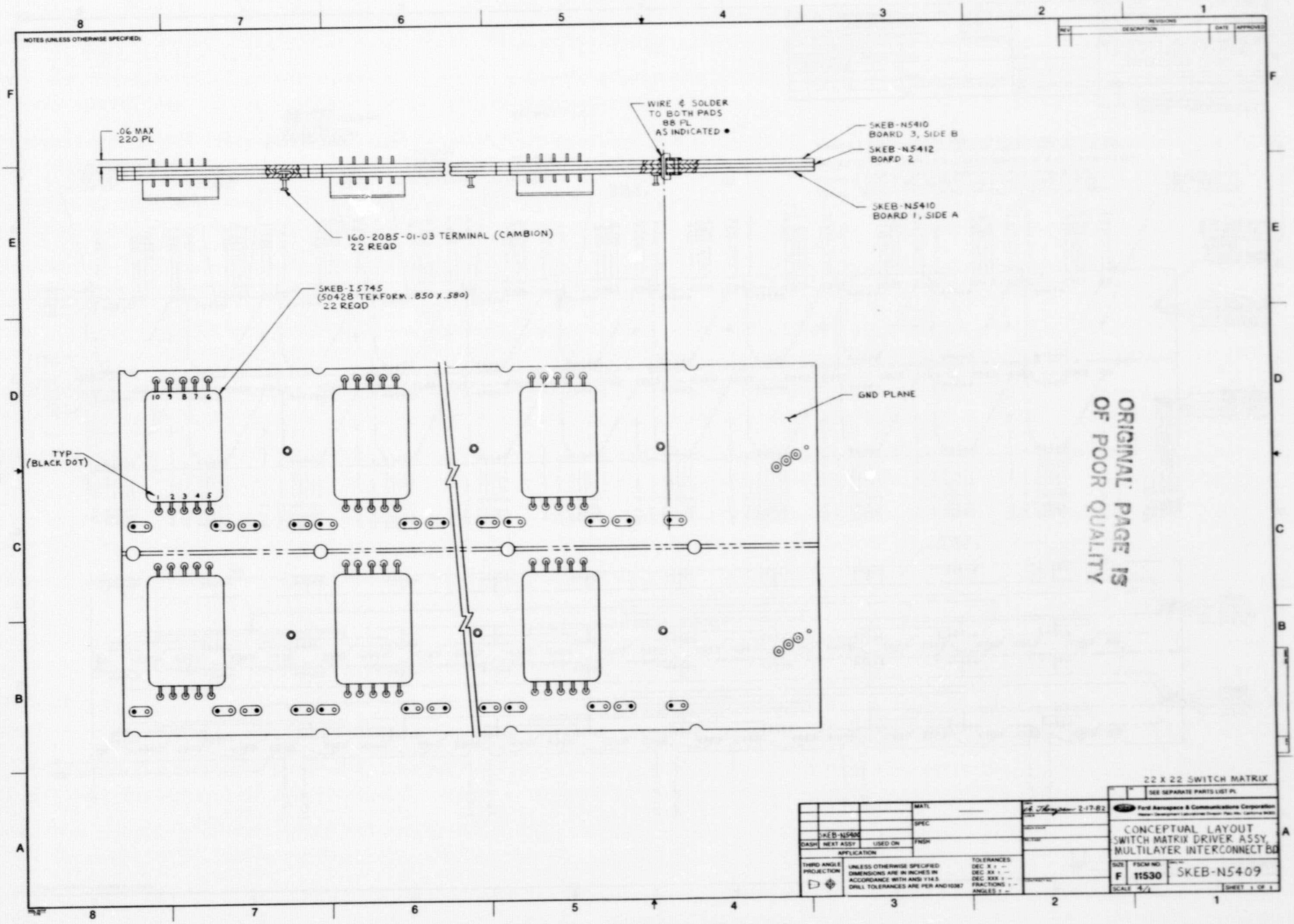

Fig. 5.6 Switch Driver PC Board

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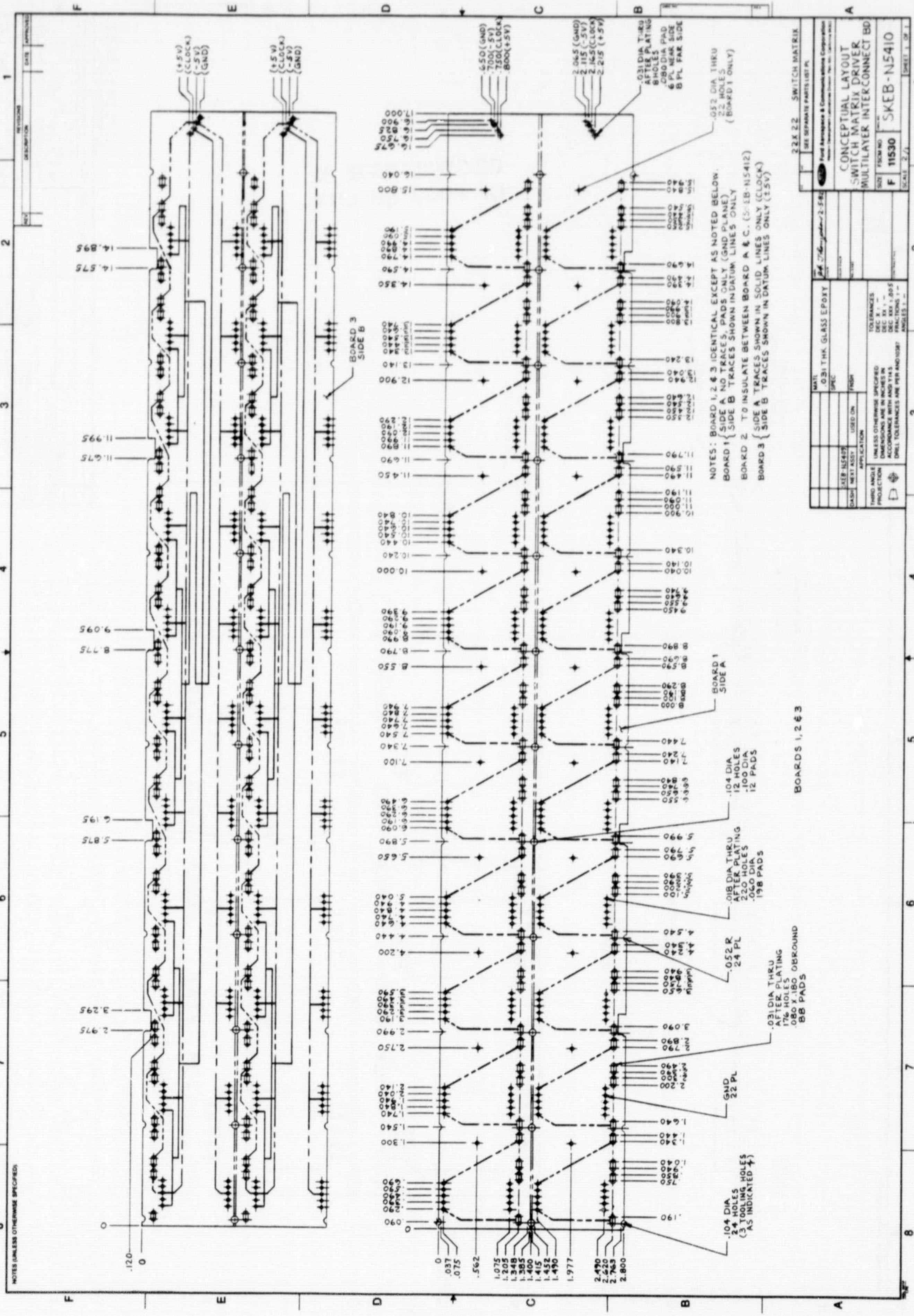
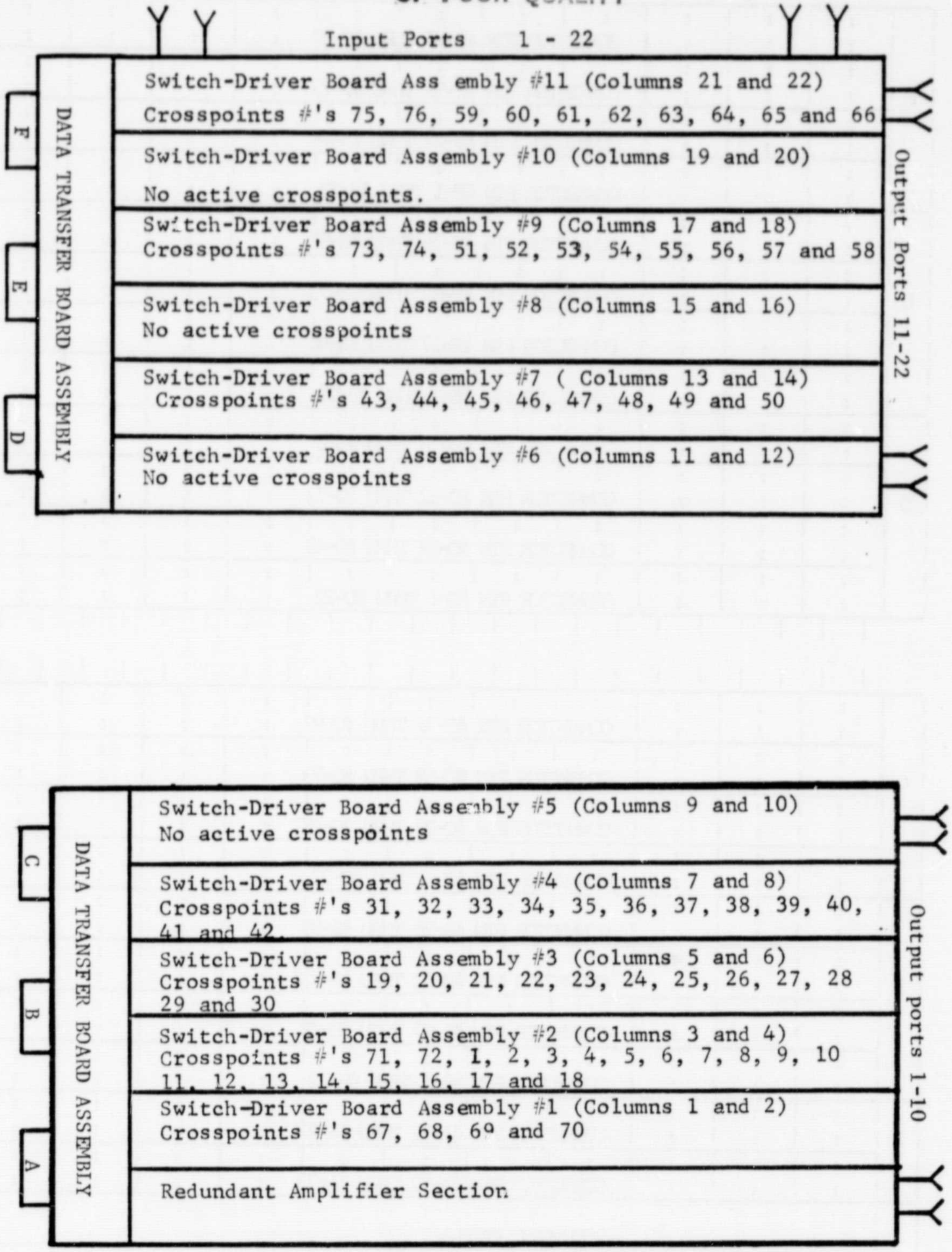


Fig. 5.7 PC Board Wiring Diagram



Switch-Driver P.C. Board Assemblies

Fig. 5.8

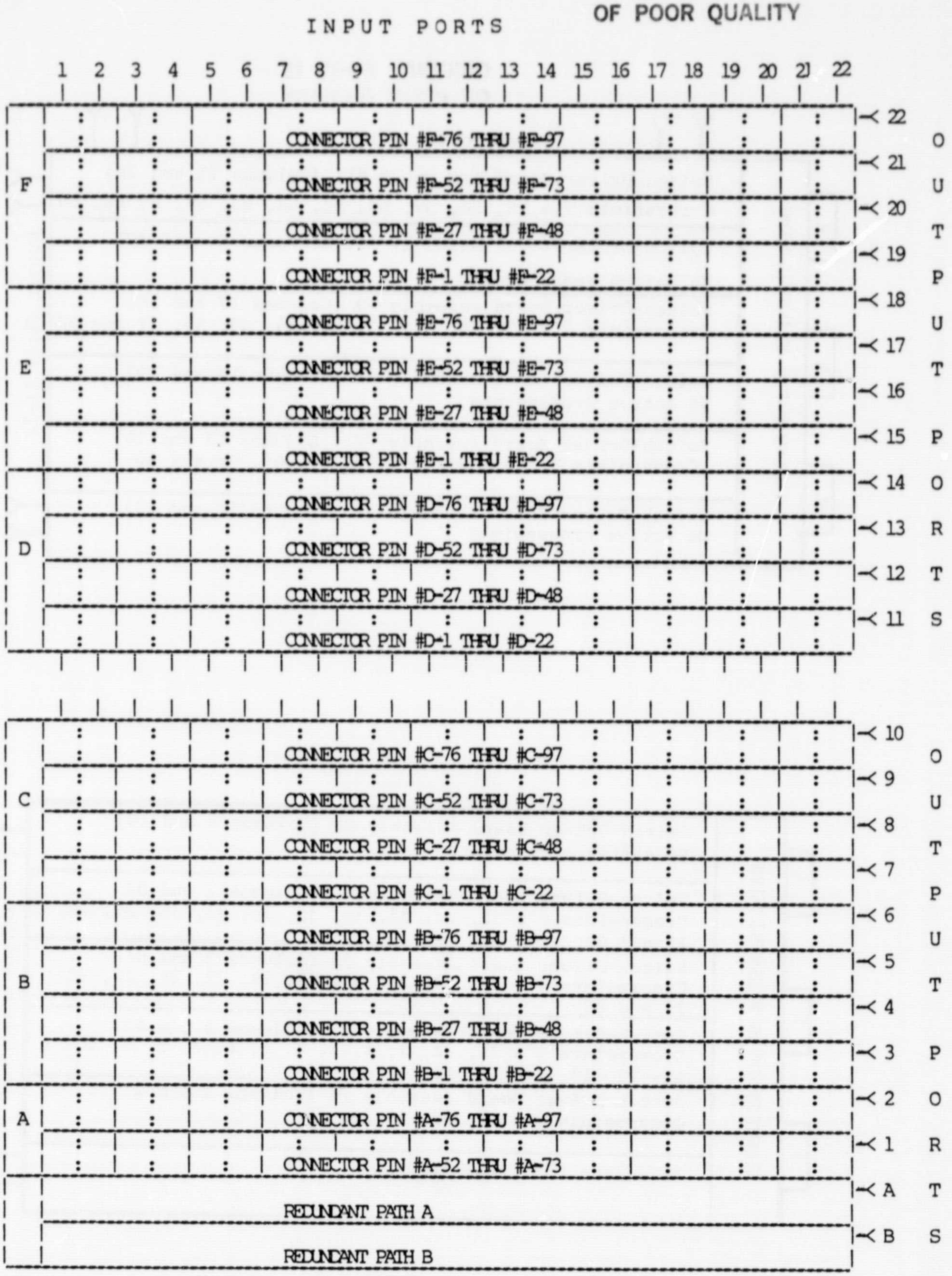


Fig. 5.9

MSM Pin Location Diagram

lation of input and output couplers with silver-epoxy preforms using special alignment and holding down tools.

A summary of the steps used to assemble the unit is the following:

1. Install feedthrus
2. Install input and output couplers
3. Install input coupler covers
4. Install and bond 50 ohm through transmission line carriers
5. Install input and output connectors
6. Test input/output coupler insertion loss for each crosspoint of the matrix
7. Remove 50 ohm transmission line carriers
8. Install switch driver board assemblies
9. Install data transfer board
10. Install connectors and RFI/EMI filters
11. Solder and interconnect DC, data, and data transfer signals
12. Test switch drivers and output voltages for the switch amplifier modules.
13. Install switch amplifier modules biasing substrate assemblies, and redundant amplifiers.
14. Align and tune each crosspoint
15. Install switch amplifier module covers
16. Mount together top and bottom chassis, install covers, and install interconnect semi-rigid cables
17. Perform acceptance tests

6.0 DISTRIBUTION CONTROL UNIT (DCU)

The distribution control unit has been designed to exercise control over a communication switch matrix consisting of 484 crosspoints even though only 76 active crosspoints are provided for the proof-of-concept model. The control is exercised by a preprogrammed memory. Sequential readout of memory contents determines a sequence of switching configurations connecting 20 input ports with 20 output ports. Two spare paths are provided for redundancy. The sequence is repeated over a time interval called a frame.

6.1 Block Diagram

A block diagram of the DCU is shown in Figure 6.1. It consists of the following functional blocks:

1. Oscillator and countdown chain
2. Frame Sync Generator
3. Memory
4. Memory Address Counter
5. State Duration Counter
6. Sequential Pulse Generator
7. 22 Decoders

6.2 The task of each functional component is described below:

- Countdown Chain

It starts with a 4 MHz oscillator and provides the following frequencies: 4 MHz for the sequential pulse generator, 2 MHz for the state duration counter, 1 MHz and 1 KHz for the frame sync generator and any

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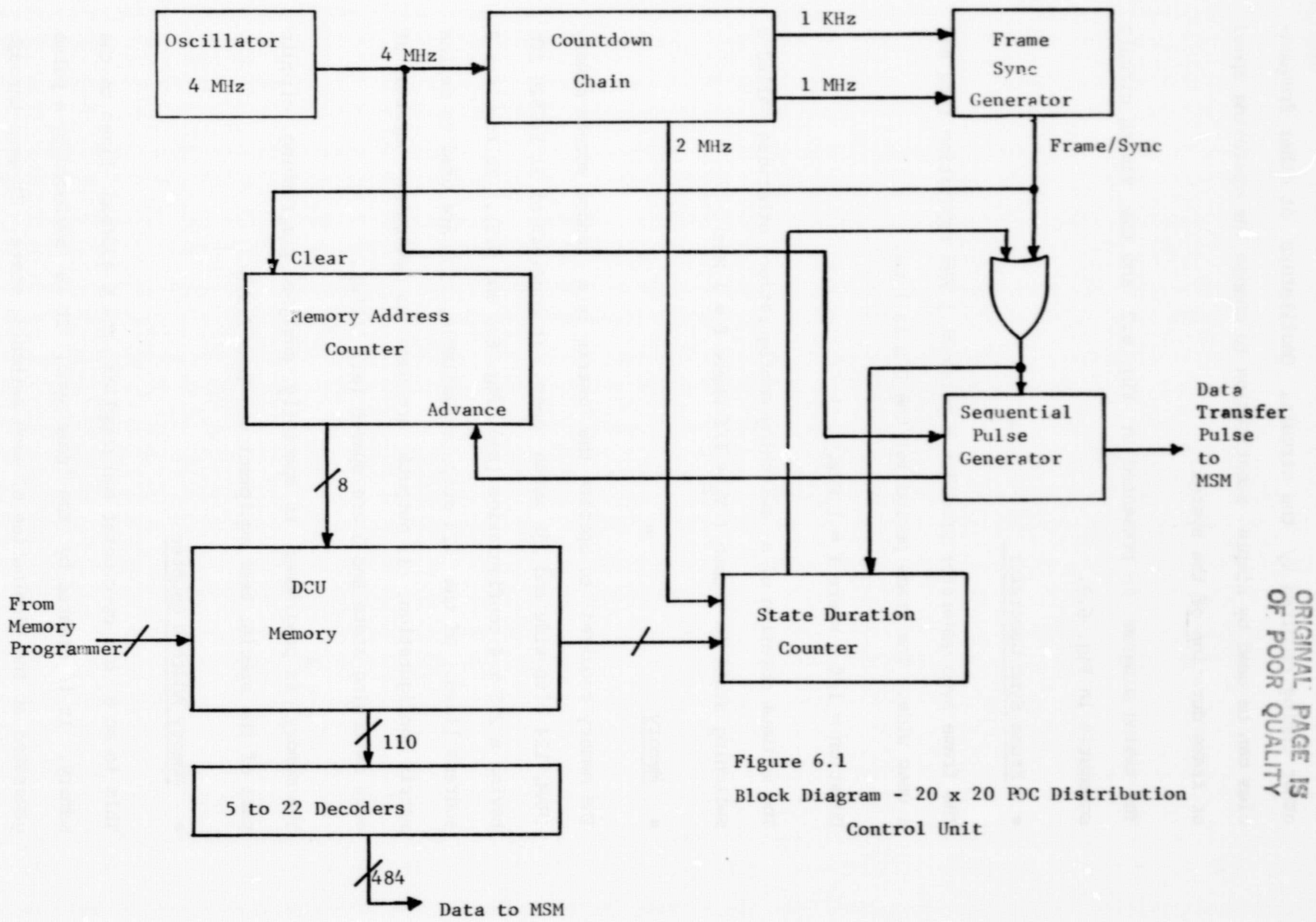

Figure 6.1
Block Diagram - 20 x 20 POC Distribution
Control Unit

other timing required by the circuit. Oscillators at other frequencies can be used by simple substitution to change the operating speed or frame duration of the system.

The timing diagram is presented in Fig. 6.2 and the timing circuit schematic in Fig. 6.3.

- Frame Sync Generator

The frame sync generator provides a pulse at 1 KHz repetition rate and 1 usec wide. The frame period for the DCU is 1 ms.

Duration = 1/f , where f = 1 KHz.

The minimum duration of a switching configuration, otherwise called a switching state is 1 usec (T_2 = 1/f where f = 1 MHz).

- Memory

The memory required to operate the matrix is a random access memory (RAM, 124 bits wide and 256 words deep. It consists of 31 54C920 ICs having a 256 x 4 configuration (see Fig. 6.4 and 6.5). It requires 8 address lines. Of the 124 outputs available, 110 are used to define matrix configuration, 11 outputs are used to determine duration of each switching state and 3 are spares (all 111's).

The memory is programmed by specially designed programming circuit part of the special test equipment see Task 2.5.3).

- Memory Address Counter

This is an 8 bit up-counter and supplies the 8 address lines to the memory. It is cleared by the frame sync. It is advanced by a pulse generated at the termination of each switching state. It goes through

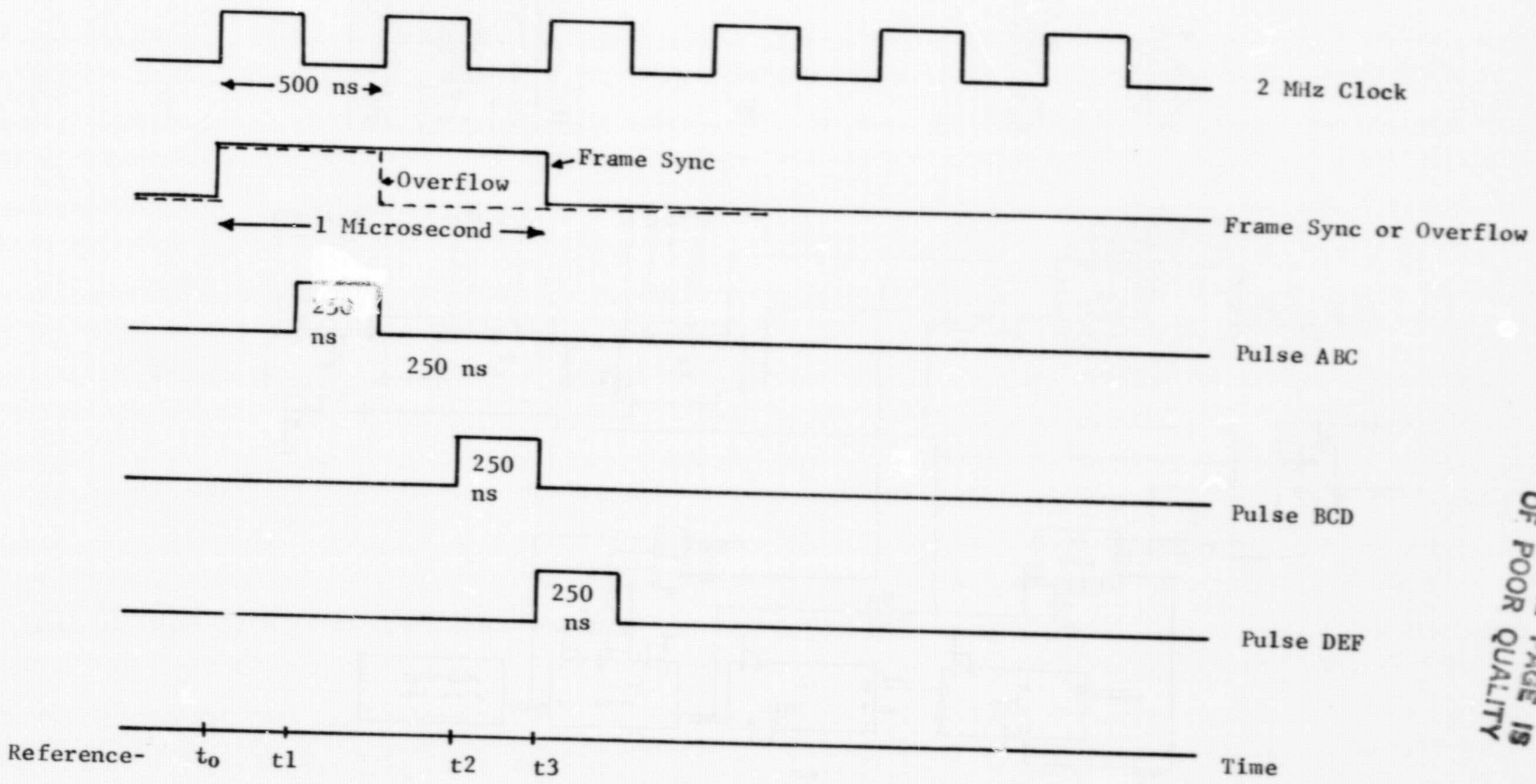

Figure 6.2 Timing Diagram of Pulses for the S.T. Generator

20 X 20 SWITCH MATRIX TIMING CIRCUIT

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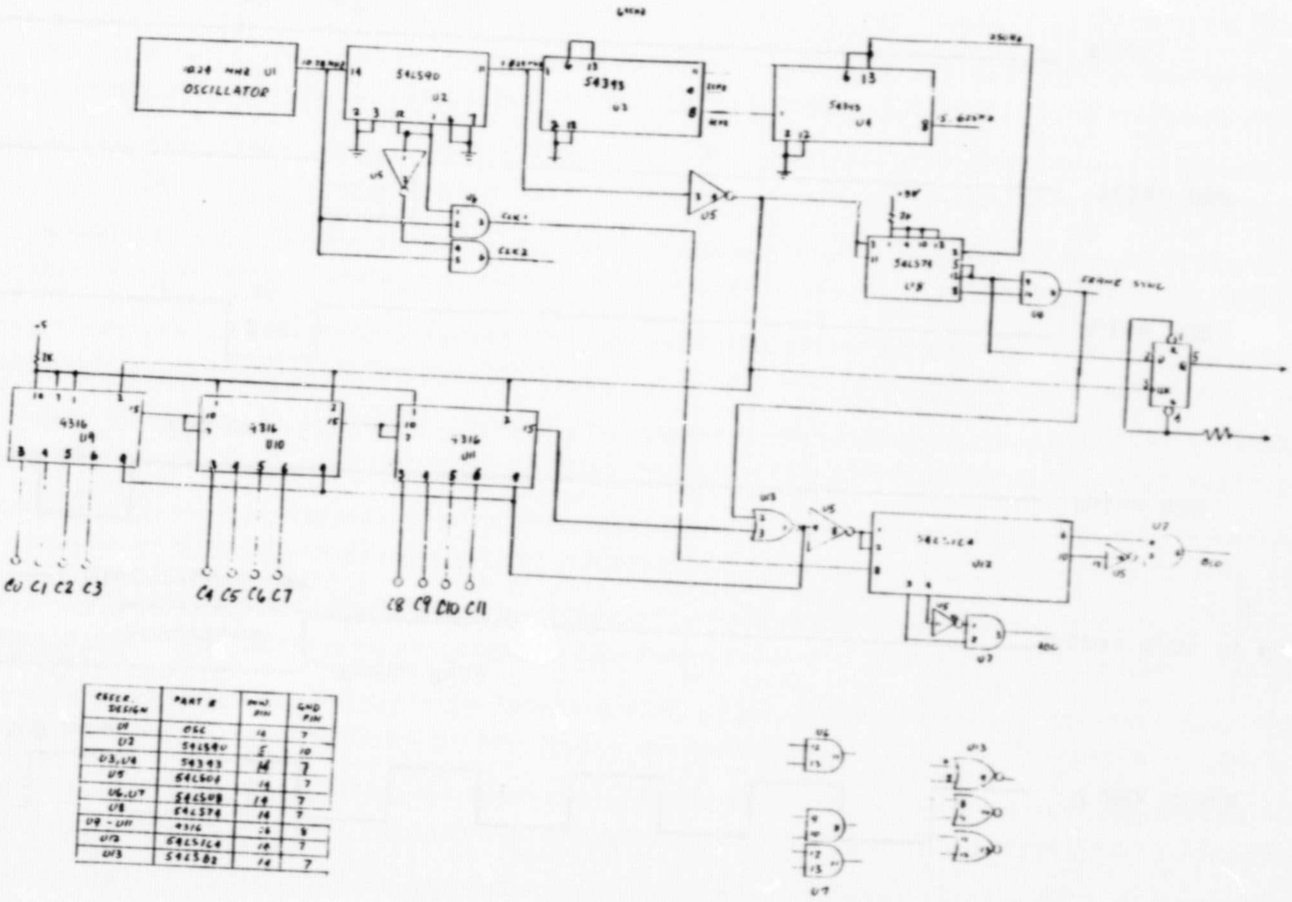

[illegible] DESIGN	PART #	PWR PIN	GND PIN
U1	OSC	14	7
U2	54LS90	5	10
U3, U4	54393	14	7
U5	54LS04	14	7
U6, U7	54LS08	14	7
U8	54LS74	14	7
U9 - U11	4316	16	8
U12	54LS164	14	7
U13	54LS02	14	7

Fig. 6.3

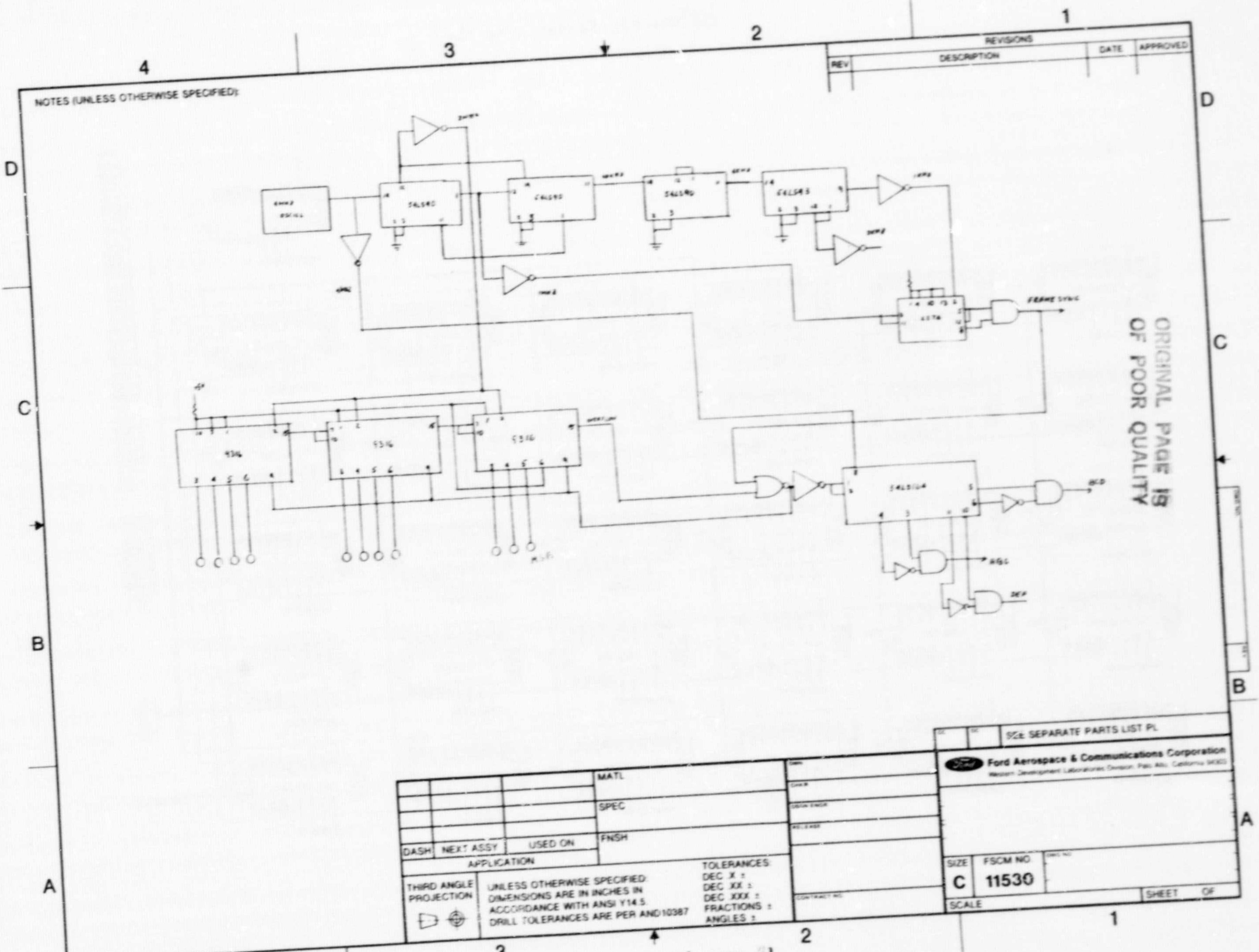

Fig. 6.4 Memory Diagram #1

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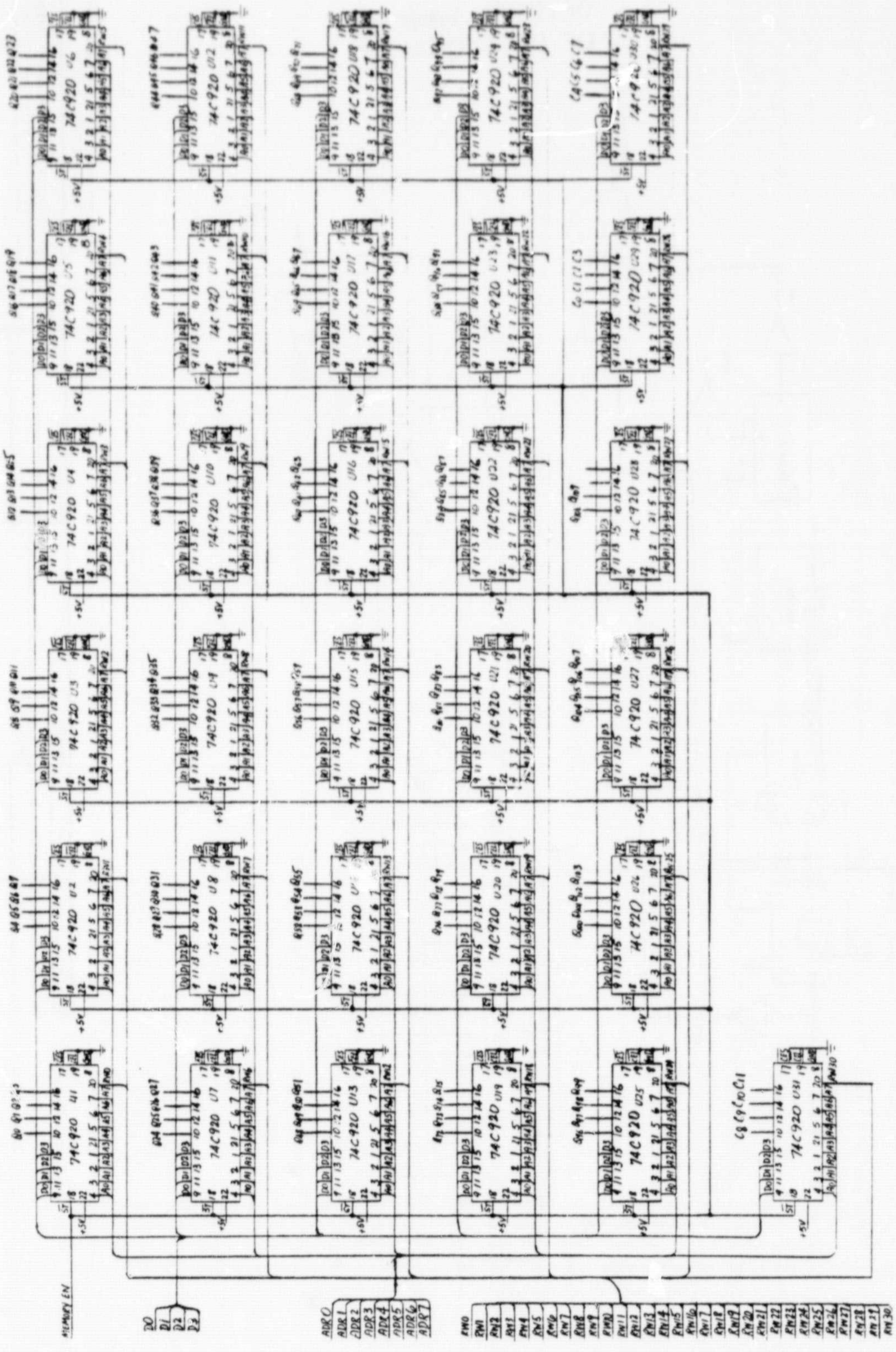

Fig. 6.5 Memory Diagram #2

all possible 256 states if the sum of all switching state durations adds up to 1m sec or less. Otherwise, the frame sync will clear the counter before all states are reached. (see Fig. 6.6)

- State Duration Counter

This is an 11 stage up-counter which determines the duration of a state. It is preloaded at the termination of each switching state by an 11 bit number from memory. When preloaded with a number N, it takes 2048-N clocks for the counter to reach overflow (all ones state). Since the clock frequency advancing this counter is 2 MHz, the duration of a state is (2048-N)/2 microseconds where N is the preloaded state duration.

- Sequential Pulse Generator

The sequential pulse generator generates a series of pulses referenced in time to an input. Each pulse follows the other in intervals of n input clock periods of 250 nsec. Each pulse is also 250 nsec wide. The pulses are used to advance the memory address counter and to transfer data from memory to the switch drivers.

The reference inputs to the pulse generator are the frame sync or the overflow from the state duration counter.

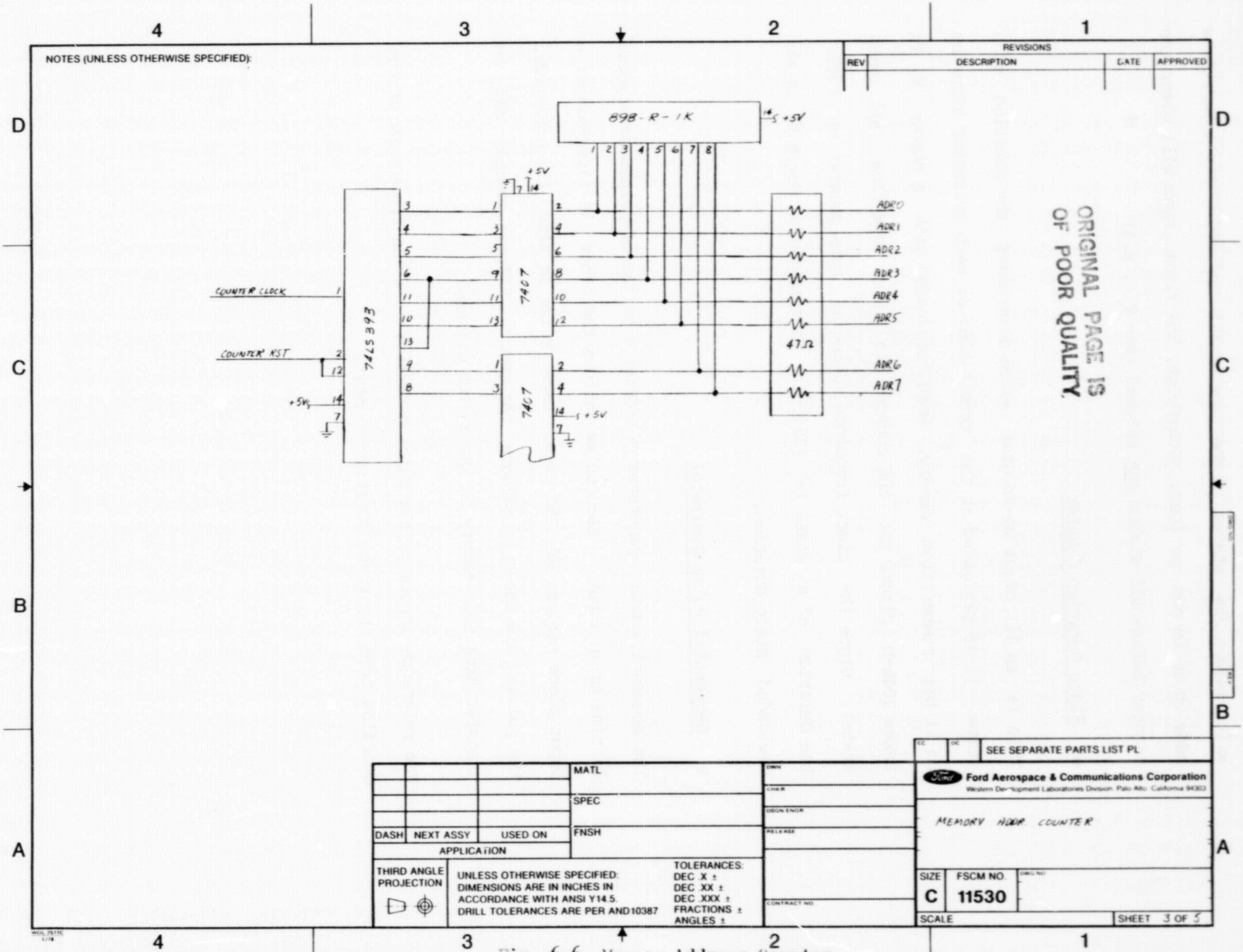

Fig. 6.6 Memory Address Counter

- <u>Decoders</u>

There are 22 decoders in the DCU (see Figs. 6.7 and 6.8). Each decoder controls one of the 22 columns. A decoder requires 5 inputs from memory and provides 22 outputs, one of which is active. These outputs go to the microwave switch matrix, one output for each crosspoint. A data transfer pulse from the sequential pulse generator transfers the data from the decoders to the storage elements of the switch drivers in the switch matrix.

- <u>Dynamic Circuit Operation</u>

After the desired program has been loaded into the RAM, the DCU may be switched to dynamic operation. In this mode, the memory address counter is advanced by a pulse coming from the sequential pulse generator and cleared at the beginning of each frame, every millisecond.

As may be seen from the block diagram, the sequential pulse generator receives two inputs; the frame sync from the count-down chain and the overflow from the state duration counter. The pulse generators respond to the input by generating a sequence of 3 pulses related in time to the input as shown in Figure 6.2.

The reference t_o represents the rising edge of either the frame sync or the overflow. The frame sync clears the memory address counter, the overflow does not affect the address counter directly. What these two pulses have in common is that they both cause a change in the counter output address lines at t_o and t_1 respectively; the frame sync does it directly, the overflow via the ABC pulse which advances the address counter. Note that the ABC pulse following the frame sync is ineffective because of the clear input at the address counter.

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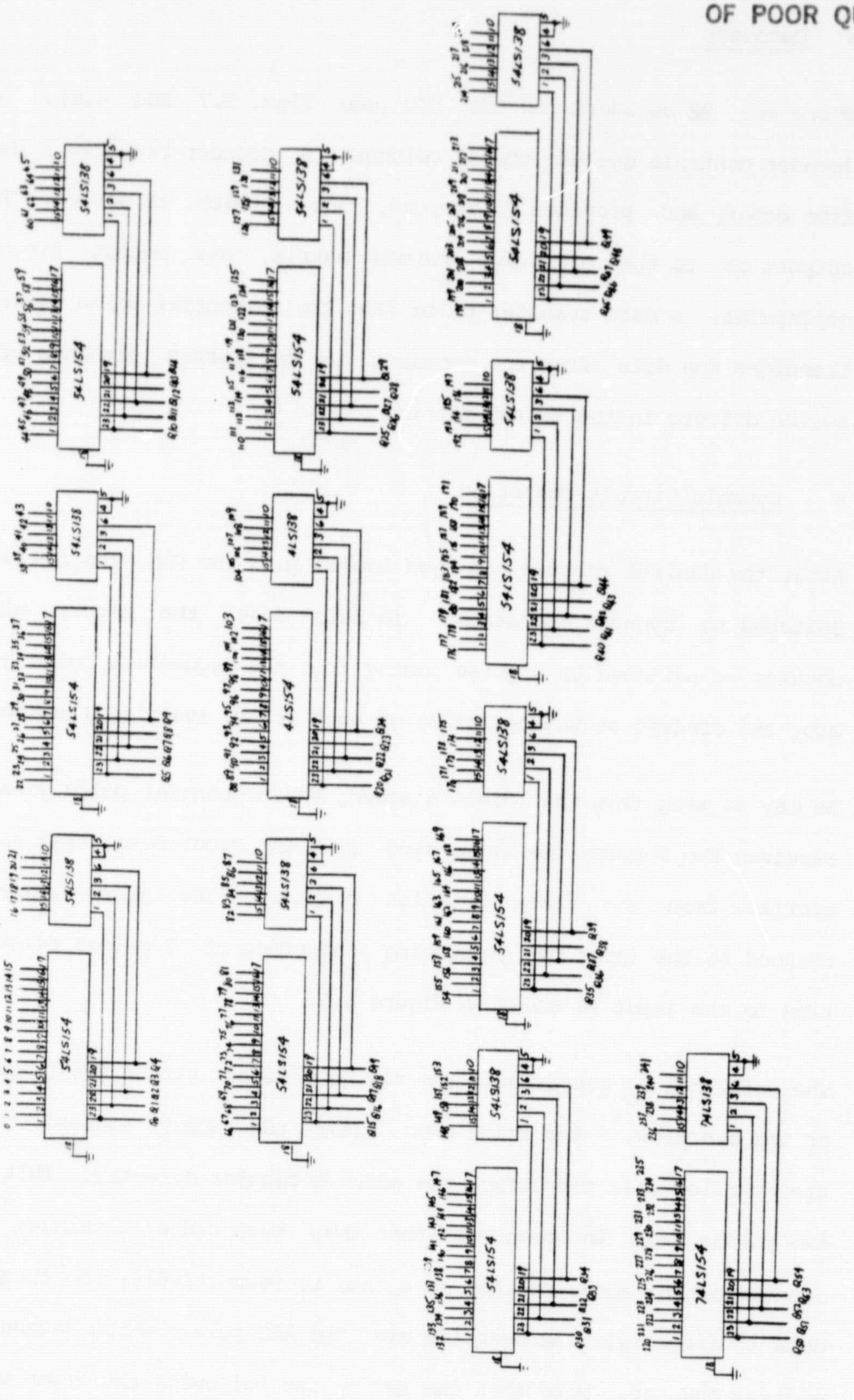

Fig. 6.7 Output Decoder I

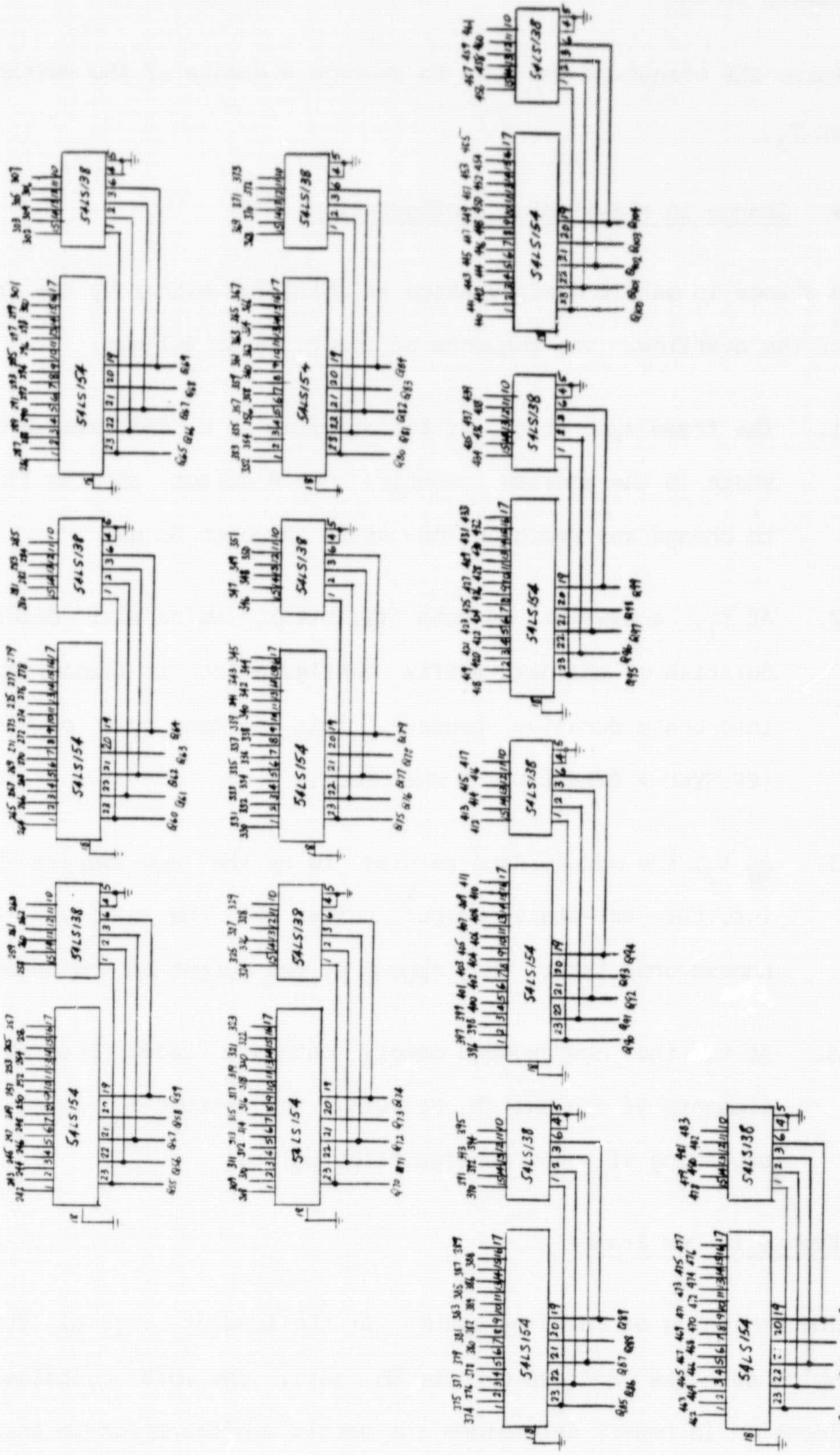

Fig. 6.8 Output Decoder II

Pulse BCD transfers the data to the tri-state output buffer of the memory at t_2.

Pulse DEF transfers the data to storage elements of the switch drivers at T_3.

- Change in a Switching Configuration

A change in matrix configuration is initiated either by the frame sync or the overflow. The sequence of events is as follows:

1. The frame sync at t_o, or the overflow at t_1 initiates a change of state in the address counter. The 8 output address lines begin to change and reach the new state in about 50 ns.

2. At t_1, a new set of data (11 bits), which will determine the duration of the next matrix configuration is loaded from memory into state duration counter. This is done by a combination of (FR.SYNC + OVERFL.). 2 MHz clock.

3. At t_2, the memory data pointed to by the new address are loaded into the tri-state output buffer of the memory. About 25 nanoseconds later, they appear at the output of the decoders.

4. At t_3, the new decoded memory data are loaded into the storage elements of the switch drivers. The instant t_3 is actually the beginning of a new configuration period.

6.3 Events in One Frame

The beginning of a frame occurs at the leading edge of frame sync, which sets the address counter to zero. The word contained at this location in memory determines the matrix configuration in this switch-

ing state and its duration T_o.

At the end of T_O, the state duration counter overflows, the memory address counter is incremented and the next state T_1 begins determined by the memory word in the new address location.

These events are repeated until all memory locations from T_o to T_{255} are stepped through and the memory address counter reverts to zero. Each stop corresponds to a separate switching state, and at most 256 states are possible. To achieve this, the following condition must be satisfied 255 T_n = 1 msec (frame period). The reason for it is that the frame sync is a forcing function and clears the address counter irrespective of the state the counter is in.

The duration of a switching state is measured in the number of clock periods advancing the state duration counter (2 MHz). The minimum duration is 2 clock periods or 1 usec, the maximum duration is a frame period or 1 msec.

A program stored in the memory gives an invariant sequence of configurations repeated every frame. To change the sequence, the memory must be reprogrammed.

The assembled DCU which includes in it the special memory load circuit is presented in Fig. 6.9. The parts list for the DCU is presented in Table 6.1.

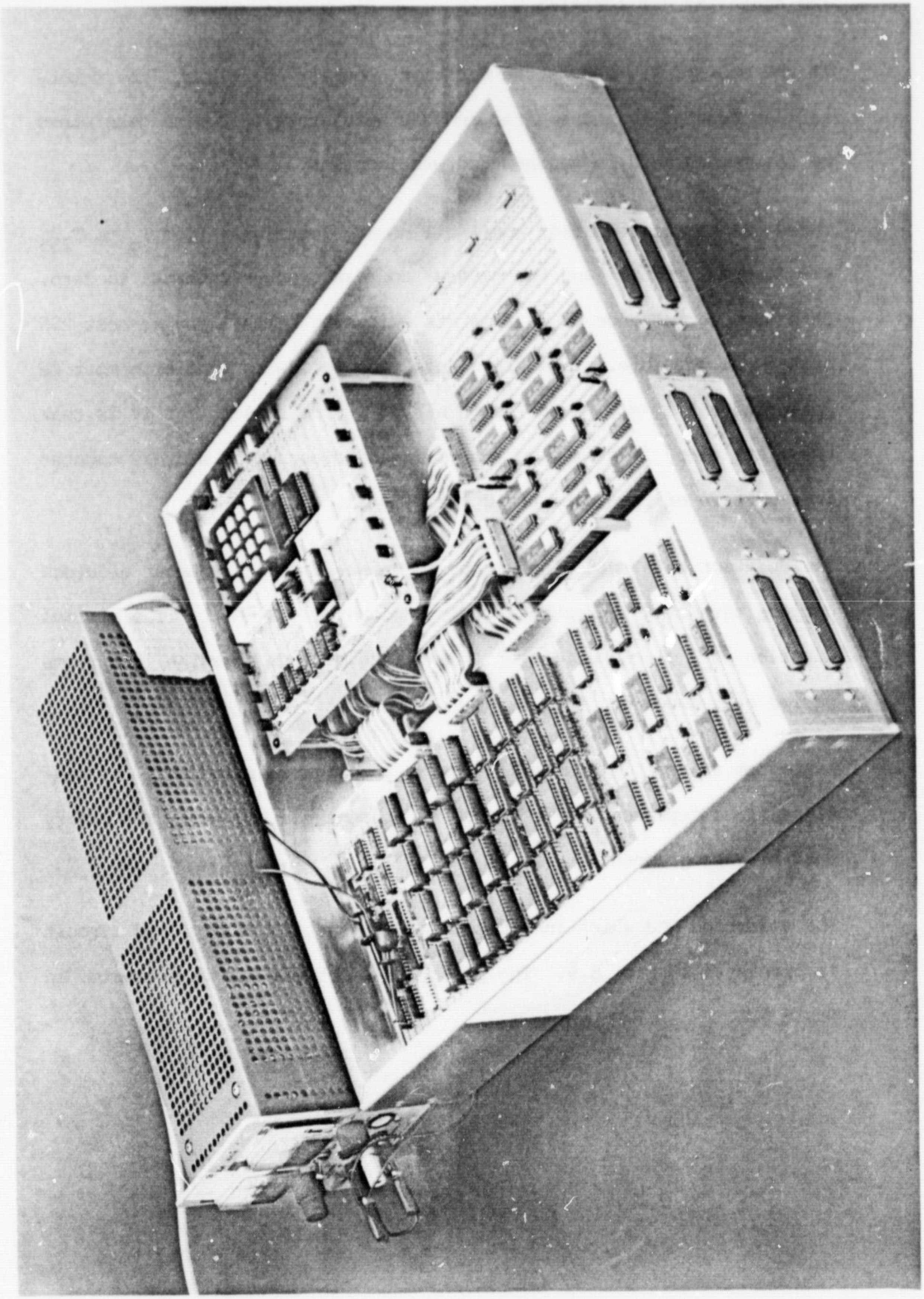

FIGURE 6.9 DISTRIBUTION CONTROL UNIT

TABLE 6.1

PARTS LIST FOR DCU

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6.4 Parts List

Description	Part Number	Quantity
2 Input NAND	54LS00	3
2 Input NOR	54LS02	2
Hex-inverter	54S04	3
Hex inverter (open collector)	54LS07	2
Counter-binary	54LS393	3
Flip flop	54LS74	2
Counter-decade	54LS90	1
3 to 8 decoder	54LS138	22
4 to 16 decoder	54LS154	22
Shift register	54LS164	1
Counter-binary	93165	5
256 x 4 CMOS memory	54C920	31
Resistive DIP	898-3-1K 899-3-47	1 1
Oscillator	C-790355 (Bliley)	1

7.0 Complete Unit

The microwave switch matrix interconnected through the six one hundred pin cables to the distribution control unit is shown in the photograph of Figure 7.1.

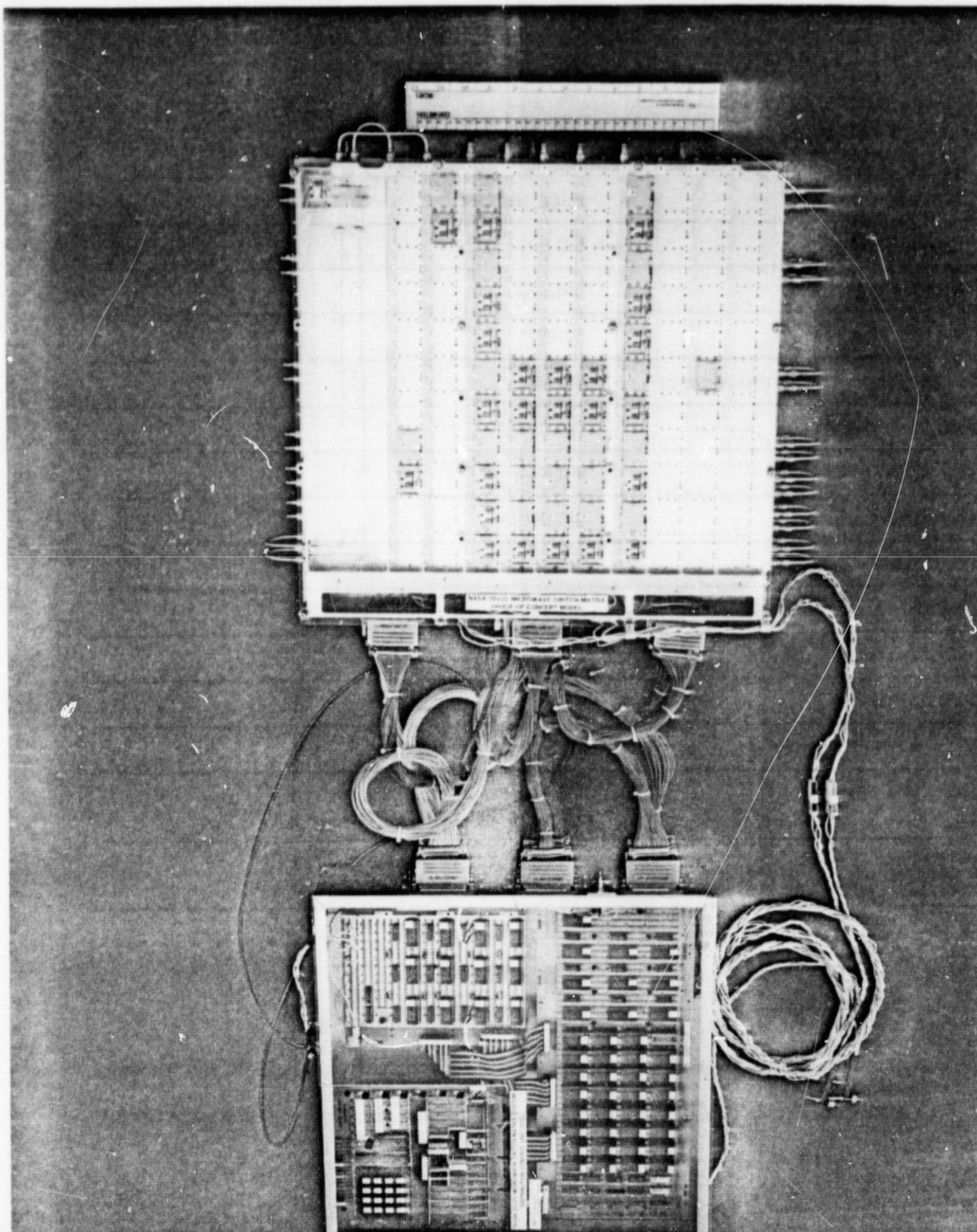

Fig. 7.1 20 x 20 MICROWAVE SWITCH MATRIX SYSTEM
(Proof-of-Concept Model)

III. POC MODEL FINAL TEST DATA

1.0 INTRODUCTION

The main objective of this section is to present the test data obtained on the 20 x 20 switch-matrix proof-of-concept model.

The testing of the POC model included functional performances and thermal-vacuum tests and was conducted at Ford Aerospace and Communications Corporation in accordance with the developed test plans and procedures. Main performance tests were conducted in the presence of Mr. E. W. Spisz, NASA Program Manager, starting November 1, 1982. All test data results and POC test analysis have been compiled in a comprehensive manner including test details, plots, test set-ups, and performance statistical analysis.

2.0 PERFORMANCE SUMMARY AND MATRIX DESCRIPTION

The POC model switch-matrix performance achieved or exceeded the desired specification in nearly all required areas. Matrix configuration included 20 inputs and 20 outputs with 76 active crosspoints spread throughout matrix. Two levels of wrap-around redundancy were included to adequately simulate continued operational capability in the event of two separate crosspoint failures. A complete summary of the matrix specifications is shown in Table 2.1 with a photo of the complete microwave matrix and distribution control unit shown in Figure 2.1. Figures 2.2 and 2.3 show the location of all crosspoints within the matrix as well as the location of the input coupler rows and the output coupler rows. Table 2.2 summarizes all crosspoint information for the 20 x 20 switch matrix including the dynamic and static DCU codes.

SPECIFICATION VS PERFORMANCE

PARAMETER		SPECIFICATION	PERFORMANCE
MATRIX SIZE		20 x 20	20 x 20
CONNECTIVITY		76 ACTIVE X-POINTS	76 12 ACTIVE INPUTS 8 ACTIVE OUTPUTS
FRAME DURATION		1 ms	1 ms
NUMBER OF STATES PER FRAME		N/A	256
RECONFIGURATION RATE		2 μs	1 μs
SWITCHING SPEED		10 ηs	5 ηs
IF FREQUENCY		3.5 TO 6.00 GHz	3.5 TO 6.0 GHz
IF BANDWIDTH		2.5 GHz	2.5 GHz
INSERTION LOSS		18 dB	20 dB
GAIN/INSERTION LOSS RIPPLE		1.0 dB PER 1 GHz	< 1 dB PER 1 GHz
PHASE LINEARITY		± 5 DEGREES	± 5 DEGREES
ISOLATION		40 dB	> 45 dB
INPUT VSWR		1.5:1	< 1.5:1
OUTPUT VSWR		1.5:1	1.5:1
INPUT SIGNAL LEVEL		-30 dBm ÷ -10 dBm	-15 dBm ÷ +10 dBm
1 dB COMPRESSION POINT		N/A	+16 dBm
MAX INPUT SIGNAL		+10.0 dBm	> +16 dBm
NOISE LEVEL (BELOW OUTPUT LEVEL)		35 dB	> 50 dB AT -5 dBm INPUT
	MATRIX	N/A	18.75" x 19" x 3.25"
	DCU	N/A	17" x 17" x 3.25"
CONSUMPTION (76 CROSSPOINTS)			
	MATRIX	N/A	5.7 WATTS
	DCU	N/A	6.25 WATTS
WEIGHT (76 CROSSPOINTS)			
	MATRIX	N/A	8.685 kg (19 lb, 3 oz)
	DCU	N/A	4.900 kg (10 lb, 13 oz)

FIGURE 2.1

Ford Aerospace &
Communications Corporation

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CROSSPOINT LOCATION DIAGRAM

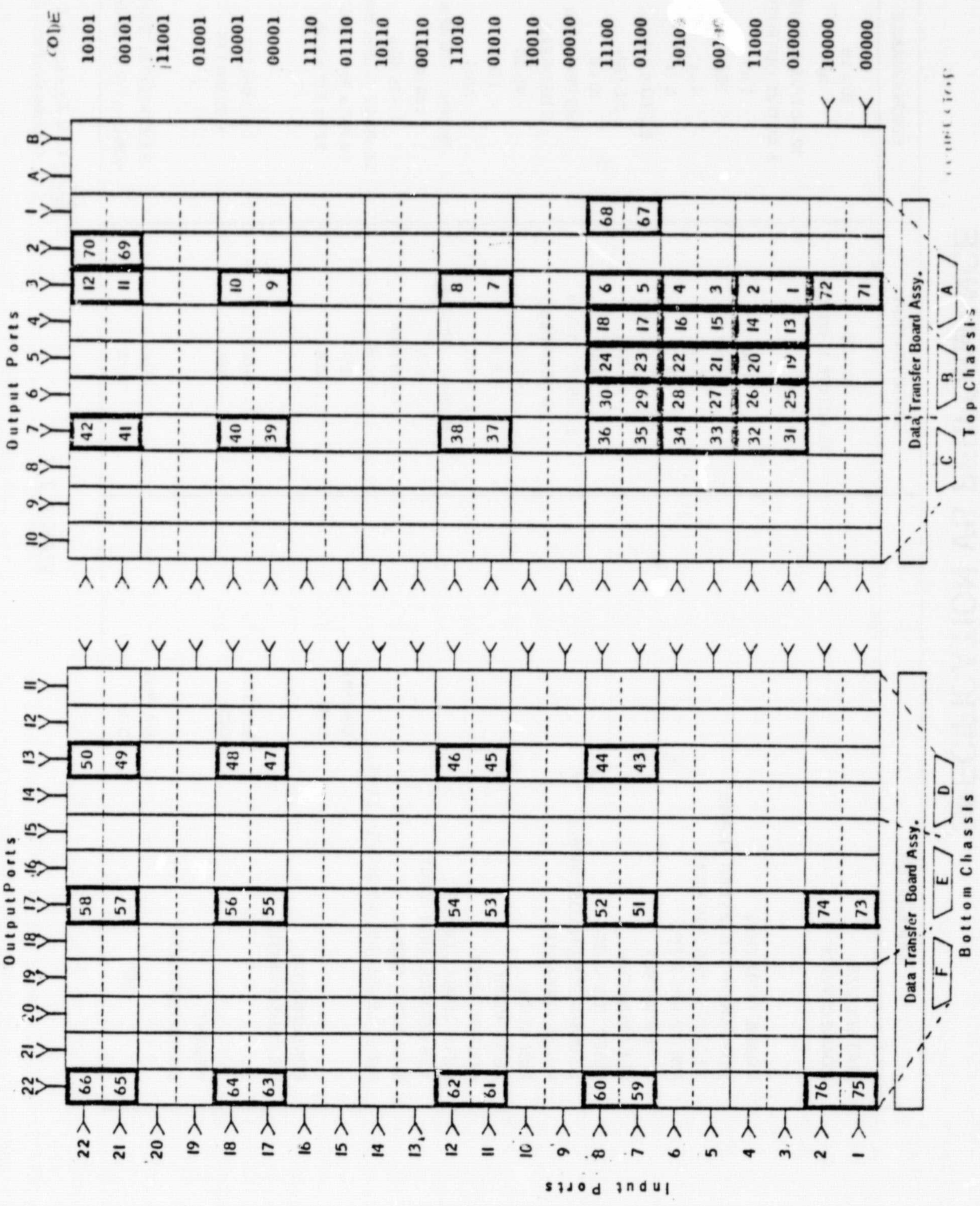

FIGURE 2.2

TABLE 2.1

MATRIX CROSSPOINTS TABLE

Cross-point #	Locat. Code In/Out	Input Port	Output Port	Sw.Ampl Module S/N	Reverse 5 dig. code	Conn. Pin #	Alternate Connection	SW DR BD
1	0303	03	03	12	01000	B-3		
2	0403	04	"		11000	B-4		
3	0503	05	"	24	00100	B-5		
4	0603	06	"		10100	B-6		
5	0703	07	"	25	01100	B-7	0701+0103/(67+71)	
6	0703	08	"		11100	B-8	0801+0103/(68+71)	
7	1103	11	"	20	01010	B-11		
8	1203	12	"		11010	B-12		
9	1703	17	"	27	00001	B-17		
10	1803	18	"		10001	B-18		
11	2103	21	"	26	00101	B-21	2102+0203/(69+72)	
12	2203	22	"		10101	B-22	2202+0103/(70+72)	2
13	0304	03	04	15	01000	B-29		
14	0404	04	"		11000	B-30		
15	0504	05	"	3	00100	B-31		
16	0604	06	"		10100	B-32		
17	0704	07	"	17	01100	B-33		
18	0804	08	"		11100	B-34		
19	0305	03	05	22	01000	B-54		
20	0405	04	"		11000	B-55		
21	0505	05	"	4	00100	B-56		
22	0605	06	"		10100	B-57		
23	0705	07	"	23	01100	B-58		
24	0805	08	"		11100	B-59		3

Cross-point #	Locat. Code In/Out	Input Port	Output Port	Sw.Ampl Module S/N	Reverse 5 dig. code	Conn. Pin #	Alternate Connection	SW DR BD
25	0306	03	06	5	01000	B-78		3
26	0406	04	"		11000	B-79		
27	0506	05	"	28	00100	B-80		
28	0606	06	"		10100	B-81		
29	0706	07	"	21	01100	B-82		
30	0806	08	"		11100	B-83		
31	0307	03	07	13	01000	C-3		
32	0407	04	"		11000	C-4		
33	0507	05	"	19	00100	C-5		
34	0607	06	"		10100	C-6		
35	0707	07	"	7	01100	C-7		
36	0807	08	"		11100	C-8		4
37	1107	11	"	6	01010	C-11		
38	1207	12	"		11010	C-12		
39	1707	17	"	16	00001	C-17		
40	1807	18	"		10001	C-18		
41	2107	21	"	8	00101	C-21		
42	2207	22	"		10101	C-22		
43	0713	07	13	41	01100	D-58		
44	0813	08	"		11100	D-59		
45	1113	11	"	39	01010	D-62		
46	1213	12	"		11010	D-63		7
47	1713	17	"	40	00001	D-68		
48	1813	18	"		10001	D-69		
49	2113	21	"	38	00101	D-72		
50	2213	22	"		10101	D-73		
51	0717	07	17	33	01100	E-58	0701+0117/(67+73)	
52	0817	08	"		11100	E-59	0801+0117/(68+73)	
53	1117	11	"	37	01010	E-62		
54	1217	12	"		11010	E-63		9

Cross-point #	Locat. Code In/Out	Input Port	Output Port	Sw.Ampl Module S/N	Reverse 5 dig. code	Conn. Pin #	Alternate Connection	SW DR BD
55	1717	17	"	36	00001	E-68		9
56	1817	18	"		10001	E-69		
57	2117	21	"	34	00101	E-72	2102+0217/(69+74)	
58	2217	22	"		10101	E-73	2202+0217/(70+74)	
59	0722	07	22	32	01100	F-82	0701+0122/(67+75)	
60	0822	08	"		11100	F-83	0801+0122/(68+75)	
61	1122	11	"	31	01010	F-86		
62	1222	12	"		11010	F-87		11
63	1722	17	"	30	00001	F-92		
64	1822	18	"		10001	F-93		
65	2122	21	"	29	00101	F-96	2102+0222/(69+76)	
66	2222	22	"		10101	F-97	2202+0222/(70+76)	
Redundant Path								
67	0701	07	01	14	01100	A-58		
68	0801	08	"		11100	A-59		
69	2102	21	02	11	00101	A-96		1
70	2202	22	02		10101	A-97		
71	0103	01	03	18	00000	B-1		2
72	0203	02	03		10000	B-2		
73	0117	01	17	35	00000	E-52		9
74	0217	02	15		10000	E-53		
75	0122	01	22	2	00000	F-76		11
76	0222	02	22		10000	F-77		

* Wraparound Amplifier : Module S/N 39

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3.0 PROOF OF CONCEPT MODEL TEST DATA

An extensive amount of testing was completed on the 20 x 20 switch-matrix POC model. A table summarizing all tests performed is shown in Table 3.1.

TABLE 3.1

POC MODEL IF SWITCH MATRIX SYSTEM
TOP LEVEL TEST PLAN

DESCRIPTION	Number of Crosspoints to be Tested (minimum)	Manual (M), Auto (A) or Semiautomatic (S) Test	Special Test Equipment	Room Conditions	Thermal Vacuum (2 X-Point Mod. only	After Thermal Vacuum Tests	Swept Measurement	Center Frequency	COMMENTS
FUNCTIONAL SWITCHING									
-CONNECTIVITY	66		x	x					Data Sheet #4
-ROUTING	66		x	x					Data Sheet #4
-RECONFIGURATION	12	x		x					Data Sheet #5
-BROADCAST	12	x	x	x					Data Sheet #6
-REDUNDANCY	4	x		x			x		Data Sheet #7
ELECTR. PERFORMANCE									
-INSERTION LOSS	66	A		x		2	x		Data Sheet
-FLATNESS	66	A		x		2	x		
-ISOLATION	66	A/M		x			x		
-BANDWIDTH	66	A		x			x		
-INPUT VSWR	66	A		x			x		
-OUTPUT VSWR	10	A/M		x			x		Data Sheet #13
-1-DB COMPRESS	4	S		x				x	Data Sheet #8
-PHASE LINEARITY	4	S		x			x		Data Sheet #8
-DC INPUT IF MX		M		x	x	x			Data Sheet #2
-DC INPUT DCU		M		x	x	x			Data Sheet #2
-SWITCHING SPEED	6	M		x				x	Data Sheet #3
-STABILITY,SPURS	66	M*		x					Data Sheet #10
-NOISE	4	M		x				x	Data Sheet #9

Note: See Data Sheet #12 for thermal-vacuum test results.
See Data Sheet #1 for matrix outline, weight, size,etc.

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3.1 Mechanical and DC Power Specifications

Section 3.1.1 outlines all major mechanical specifications for the 20 x 20 switch-matrix POC model. These specifications include size and weight parameters as well as a detailed drawing of the microwave switch matrix. Section 3.1.2 provides detailed DC power consumption in various matrix modes of operation, including the Broadcast Mode.

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3.1.1

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #1

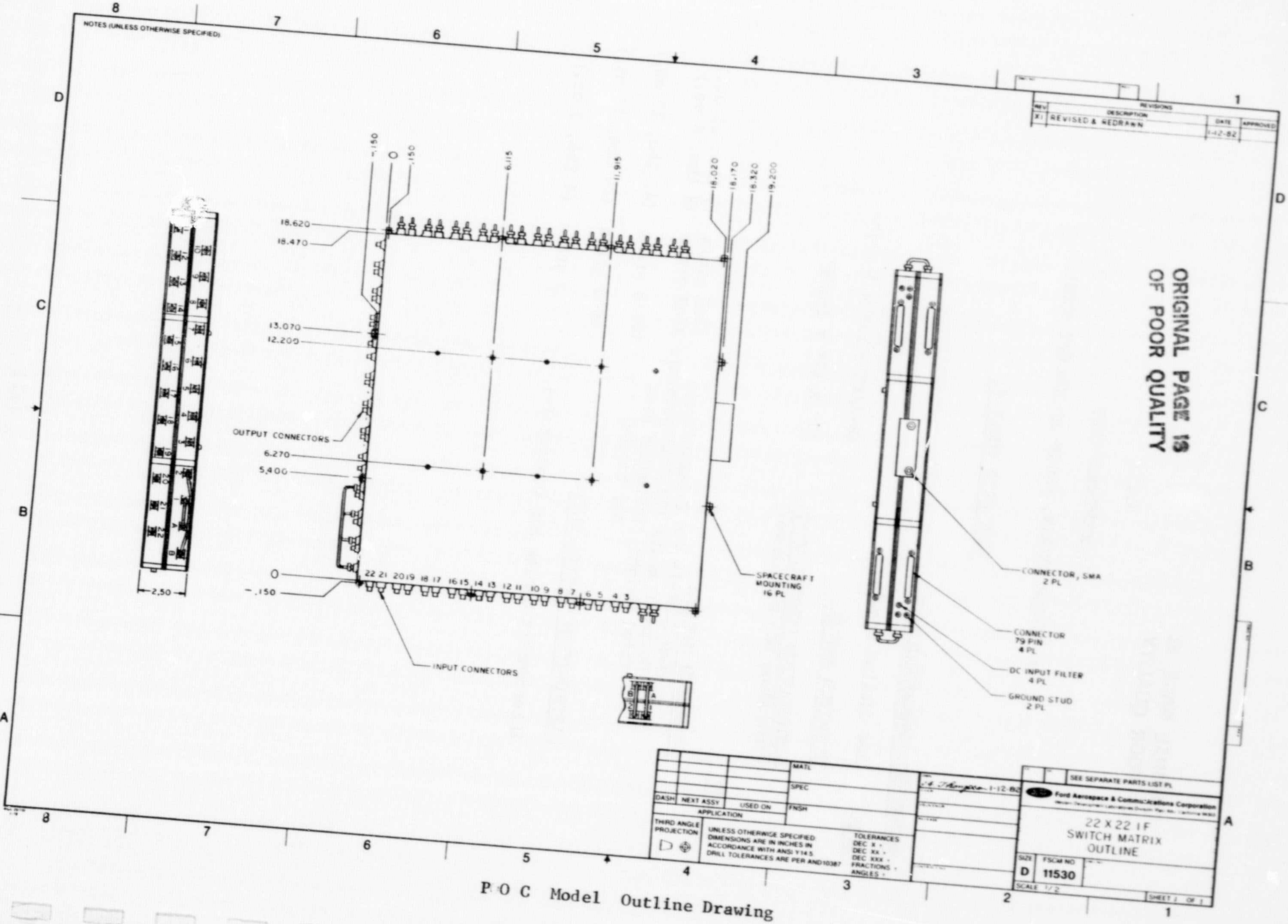
MECHANICAL CHARACTERISTICS

SIZE: See Outline Drawing

IF SWITCH MATRIX:	18-3/4" x 19" x 3-1/4"
DISTRIBUTION CONTROL UNIT: (including DCU Programmer)	17" x 17" x 3-1/4"

WEIGHT

IF SWITCH MATRIX:		
Top Chassis (48 Crosspoints):	4385 grams	(9 Lbs, 11 oz.)
Bottom Chassis (28 Crosspoints):	4300 grams	(9 Lbs, 8 oz.)
Total Weight (including base and covers) :	19335 grams	(42 Lbs, 10 oz.)
DISTRIBUTION CONTROL UNIT:	4900 grams	(10 Lbs, 13 oz.)
Interconnect Cables and Connectors:	1.910 grams	(4 Lbs, 3 oz.)



POC Model Outline Drawing

3.1.2

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #2

POWER CONSUMPTION
Summary
See Table 3.1.2.1

SWITCH MATRIX:

a. All crosspoints "OFF"

Top Chassis*	285 mA @ +5.0 Vdc
	87 mA @ -5.2 Vdc
Bottom Chassis**	91 mA @ +5.0 Vdc
	67 mA @ -5.2 Vdc
Total	376 mA @ +5.0 Vdc
	154 mA @ -5.2 Vdc

b. Fully Operational Matrix ***

Top Chassis (5 X-Points):	600 mA @ +5.0 Vdc
	123 mA @ -5.2 Vdc
Bottom Chassis (3 X- Points):	315 mA @ +5.0 Vdc
	87 mA @ -5.2 Vdc
Top and Bottom Chassis: (Total)	915 mA @ +5.0 Vdc
	210 mA @ -5.2 Vdc

DISTRIBUTION CONTROL UNIT

a. DC Current: 1200 mA @ +5.0 Vdc
50 mA @ -5.2 Vdc

* 48 active crosspoints plus dual redundant amplifier module (See Note 1)
** 28 active crosspoints
*** 12 inputs, 8 outputs, no redundant paths
(average current consumption for 8 crosspoints "ON" ,static mode)
Note 1: The consumption of the dual redundant amplifier module
is: 120 mA @ +5.0 Vdc
1.8 mA @ -5.2 Vdc

POWER CONSUMPTION (Summary)

SWITCH MATRIX (78 crosspoints, fully operational, 8 crosspoints "ON", static mode, average)		4.58 watts @ +5.0 V 1.09 watts @ -5.2 V
	TOTAL	5.67 Watts
DISTRIBUTION CONTROL UNIT		
		6.00 watts @ +5 V 0.26 watts @ -5 V
	TOTAL	6.26 watts
TOTAL CONSUMPTION		11.77 watts

Table 3.1.2.1

DC Consumption In the Broadcast Static Mode of Operation

INP	CROSSPOINTS "ON"	@ =5.0 Vdc				@ -5.2 Vdc			
		TT	BT	TOT	DCU	TT	BT	TOT	DCU
		mA	mA	mA	mA	mA	mA	mA	mA
7	5,17,23,29,35,43,51,and 59	580	345	925	1200	124	87	211	45
8	6,18,24,30,36,44,52,and 60	615	292	907	1200	123	87	211	50
21	11,41,49,57,and 65	375	285	660	1200	102	87	189	50
22	12,42,50,58,and 66	380	293	673	1200	98	86	184	48
	All Crosspoints "OFF"	285	91	376	1200	87	67	154	51

TT=Top Chassis
BT=Bottom Chassis
TOT=Total

Tested by: A. Anderson

A. Anderson

Date: 11/15/1982

3.2 Time Domain Tests

Many different time domain tests were performed to demonstrate the capability of the 20 x 20 POC Model switch-matrix to operate in a TDMA mode. Switching speed tests were performed on several different crosspoint combinations to reveal the "ON" to "OFF" and "OFF" to "ON" transition characteristics. Connectivity tests were performed on all 66 active crosspoints to insure proper dynamic and static mode operation Tests were performed to demonstrate the reconfiguration rate characteristics and also the broadcast mode of operation.

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3.2.1

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

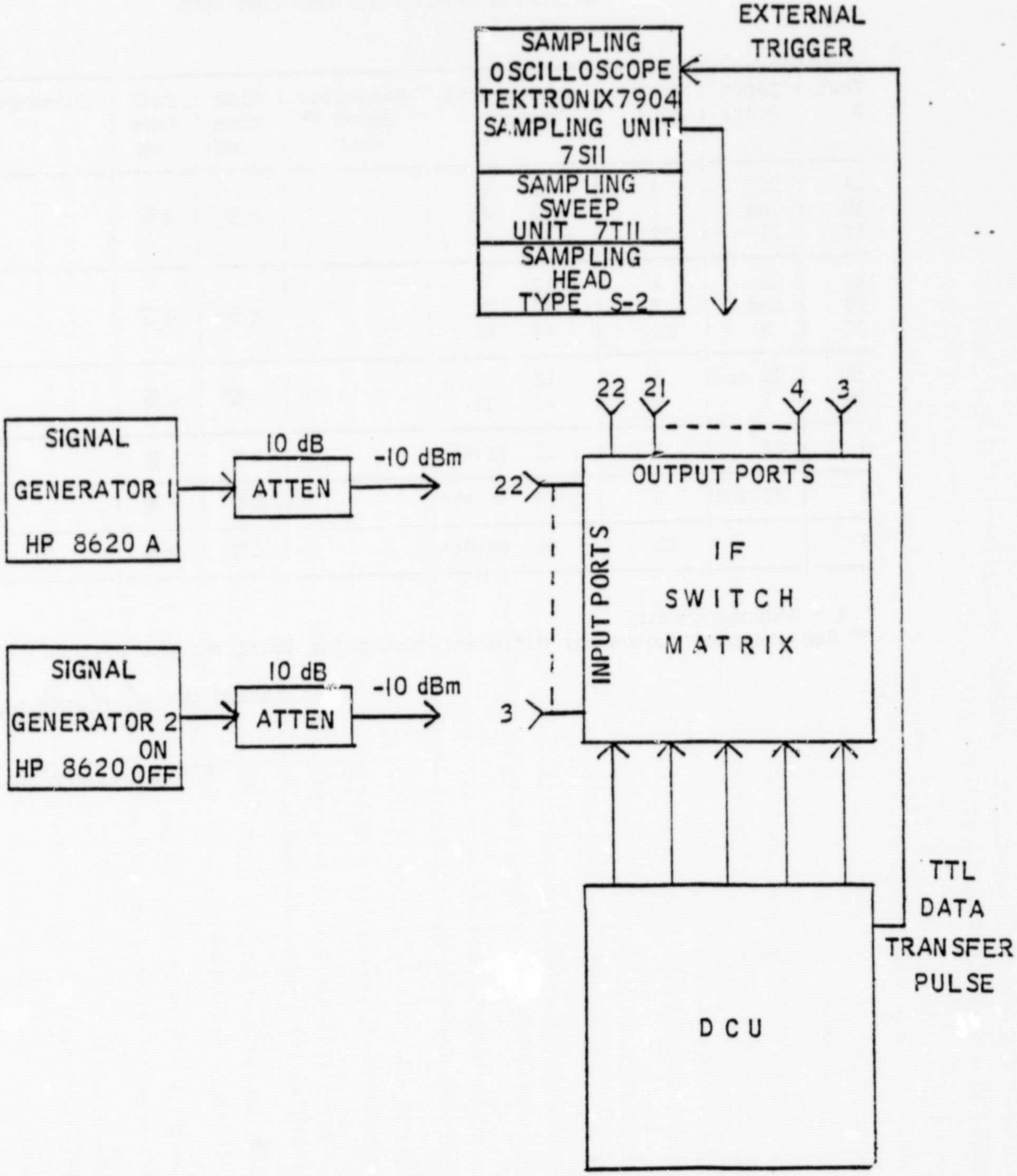
TEST DATA SHEET #3

SWITCHING SPEED TEST

Definition:	The switching speed is defined as the duration between 10% and 90% of the RF output signal voltage at the output port of the IF Switch Matrix when when a crosspoint is turned "OFF" or "ON".
Test Setup:	See Figure 3.2.1.1
Test Conditions:	Frequency 4750 MHz. RF Output Voltage: 20 mV peak (detected signal) RF Input Level: 0 dBm max.
Test Procedure:	The DCU is programmed to alternatively switch "ON" and "OFF" pairs of crosspoints on the same column of the matrix for durations of 5 us corresponding to 200 states during the lmS frame duration. The switched signal is visualized and switching speed is determined on the sampling scope screen.

Switching speed and rise and fall time durations are recorded in Table 3.2.1.1. Attach polaroid photographs. The following crosspoints will be tested: #11, 12, 41, 42, 65, 66, 6 , 36, 60, 1, Redundant #'s 6, 12 and 60.

The programming code for the 6 tests are presented in Table 3.2.1.2.



SWITCHING SPEED TEST SET UP

FIGURE 3.2.1.1

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TABLE 3.2.1.1

SWITCHING SPEED TESTS AND TEST DATA

Test #	Input Ports	Output Port	Crosspoints Tested	Reconfig. Speed ** (ns)	Rise Time (ns)	Fall Time (ns)	Comments
1A 1B 1C	22 and 21	3 7 22	12 11 42 41 66 65		<5	<5	
2A 2B 2C	22 and 8	3 7 22	12 6 42 36 66 60		<5	<5	
3A 3B	22 and 3	3 7	12 1 42 31		<5	<5	
4	22	3	12 12(R)*		<5	<5	
5	22 & 8	3	12 6(R)*		<5	<5	
6		22	66 60(R)*		<5	<5	

* R = Redundant Path
** See attached photos for different crosspoint locations and switching order.

Tested by: A. Anderson
A.Anderson

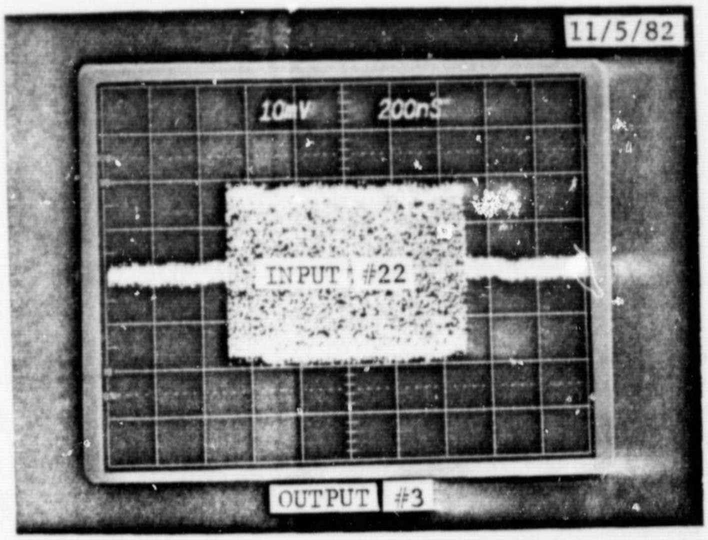
Date: 11/11/1982

TABLE 3.2.1.2

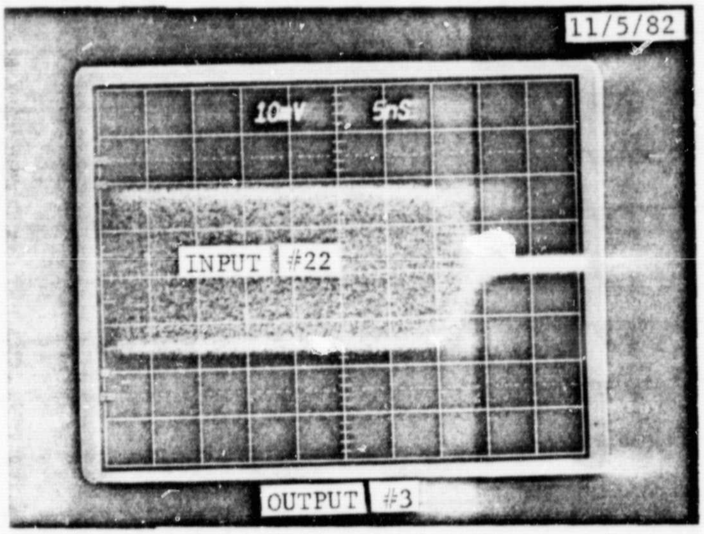
SWITCHING SPEED DCU PROGRAMMING CODES

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
66,42,12	F	F	7	D	F	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	B	E	6	F	F
65,41,11	F	F	3	D	F	F	F	3	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	9	E	6	F	F
66,42,12	F	F	7	D	F	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	B	E	6	F	F
60,36,6	F	F	F	9	F	F	F	F	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	C	6	F	F
42,12	F	F	7	[illegible]	[illegible]	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	F	F
31,1	F	F	B	8	F	F	F	B	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	F	F
12	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	F	F
12R	F	B	6	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	F	F
12	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	F	F
6R	7	E	3	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	F	F
66	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	B	E	6	F	F
60R	7	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	C	6	F	F
All Off	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0

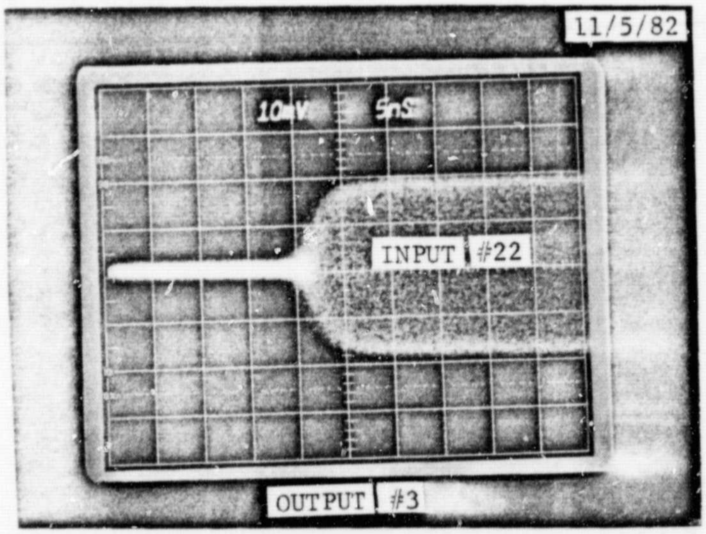
Note: 6R, 12R and 60R are redundant paths corresponding to crosspoints #'s 6, 12, and 60



STATE DURATION
1 μs "ON"
4 μs "OFF"

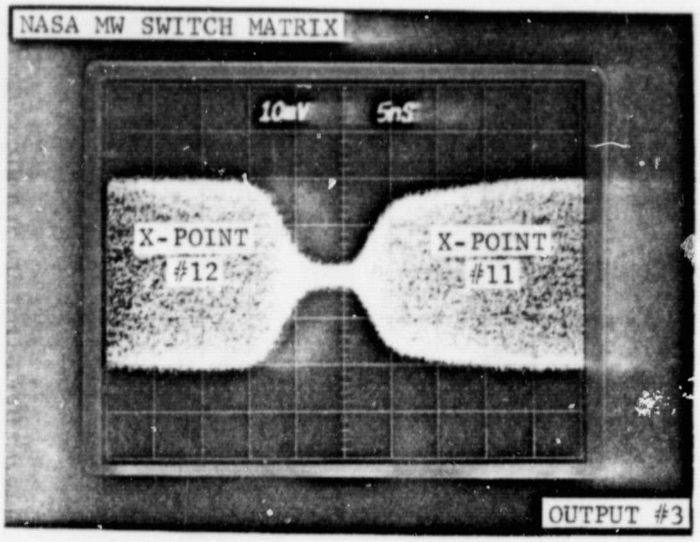


FALL TIME CROSSPOINT #12

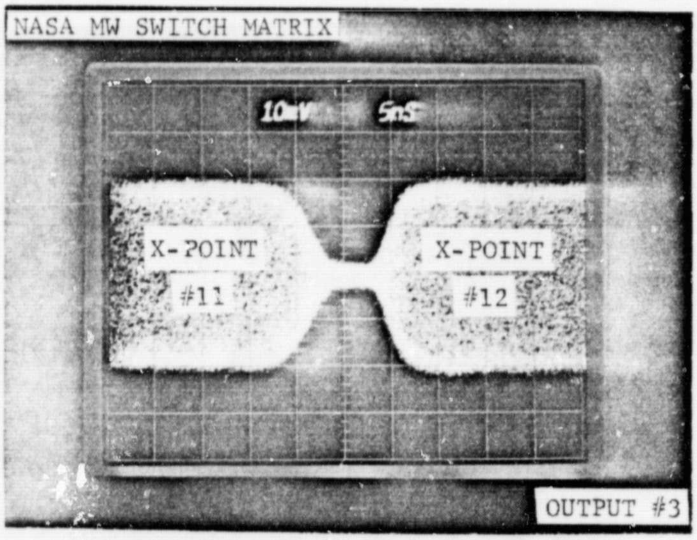


RISE TIME CROSSPOINT # 12

SWITCHING SPEED TEST

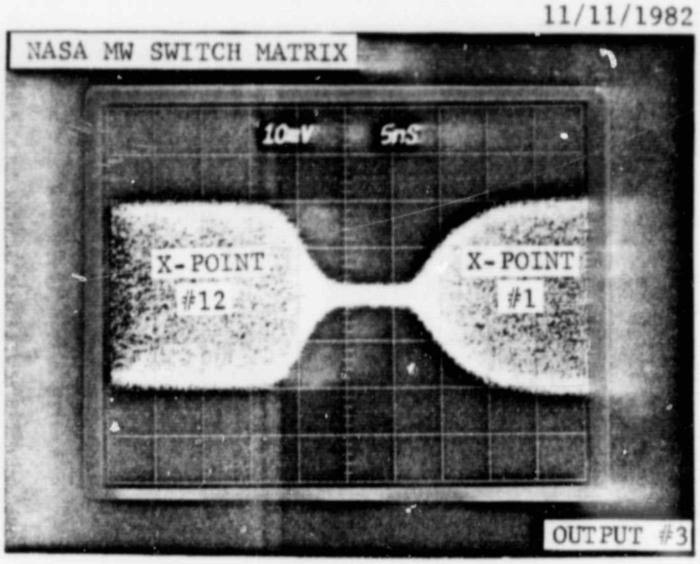


X-POINT #12 SWITCHED "OFF"
X-POINT #11 SWITCHED "ON"

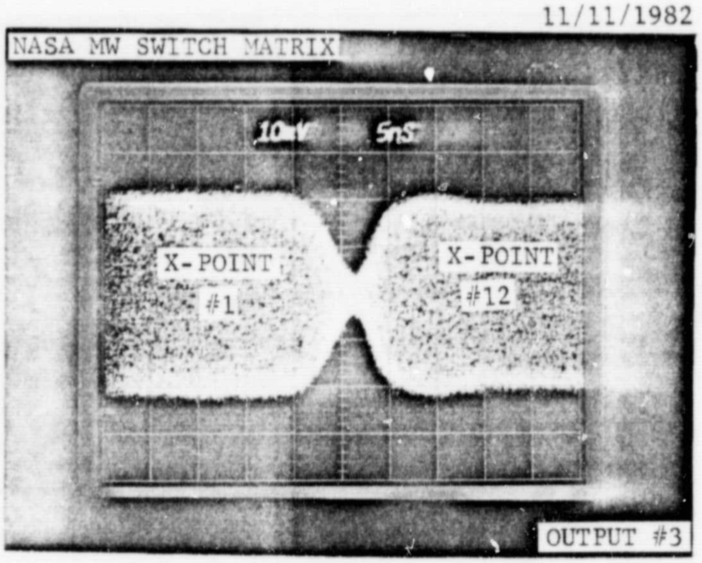


X-POINT #11 SWITCHED "OFF"
X-POINT #12 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

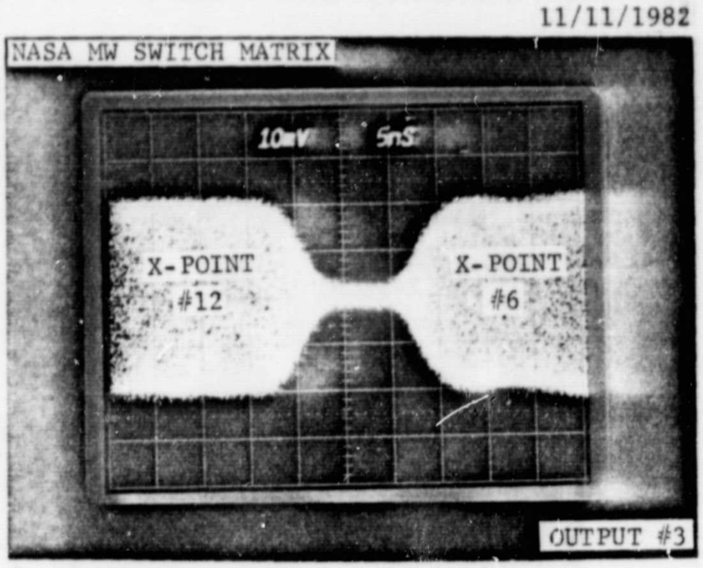


X-POINT #12 SWITCHED "OFF"
X-POINT #1 SWITCHED "ON"

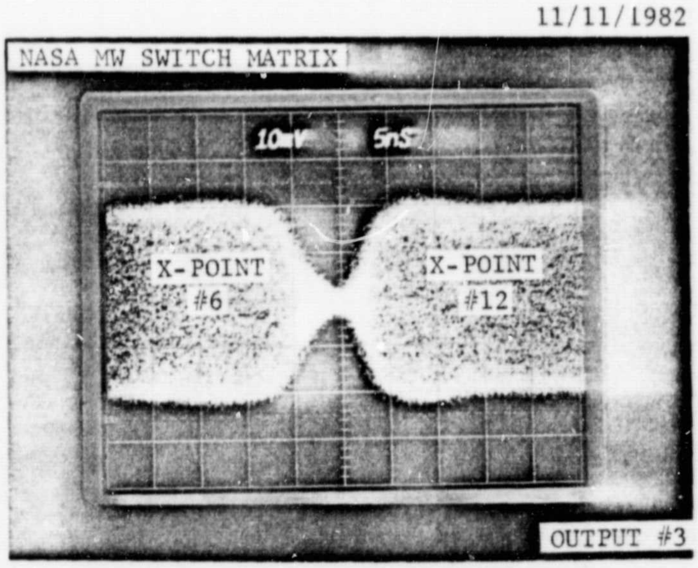


X-POINT #1 SWITCHED "OFF"
X- POINT #12 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT



X-POINT #12 SWITCHED "OFF"
X-POINT #6 SWITCHED "ON"



X- POINT #6 SWITCHED "OFF"
X- POINT #12 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

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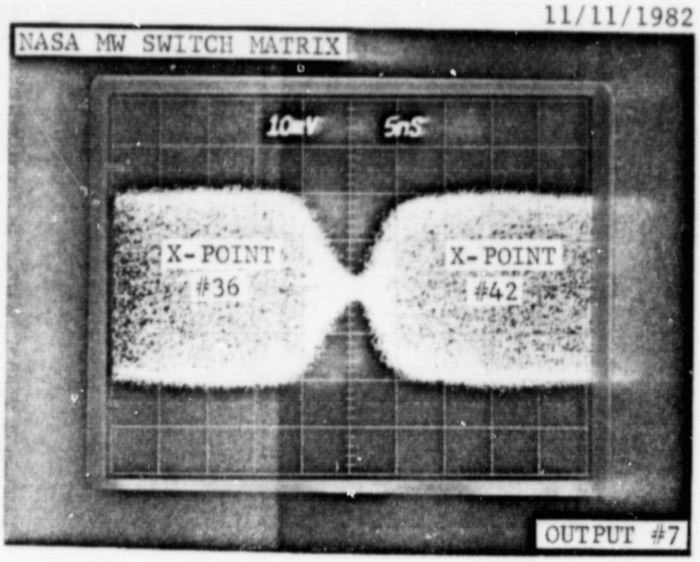
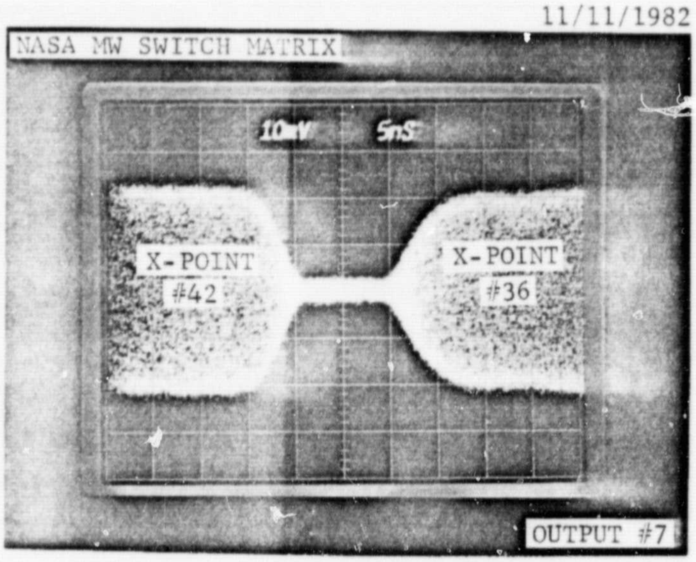
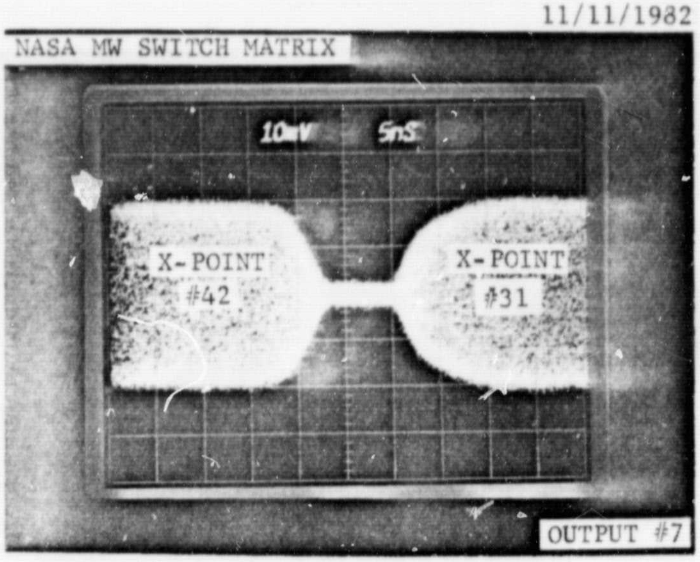


X-POINT #36 SWITCHED "OFF"
X-POINT #42 SWITCHED "ON"

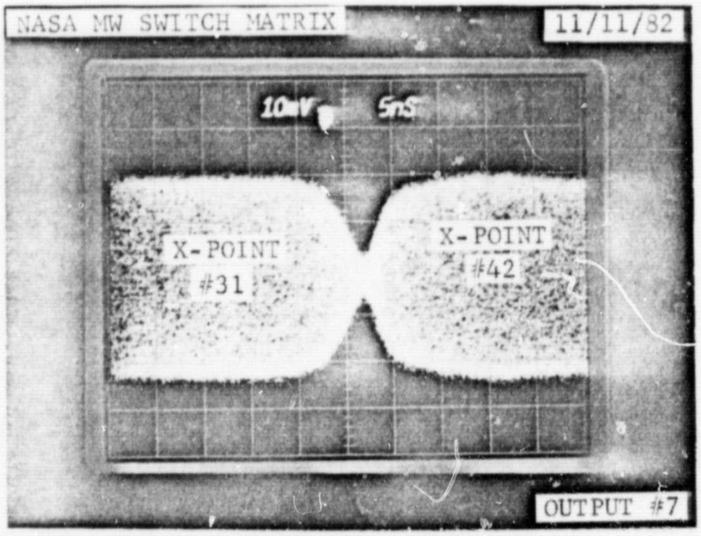


X-POINT #42 SWITCHED "OFF"
X-POINT #36 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT



X-POINT #42 SWITCHED "OFF"
X-POINT #31 SWITCHED "ON"



X-POINT #31 SWITCHED "OFF"
X-POINT #42 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

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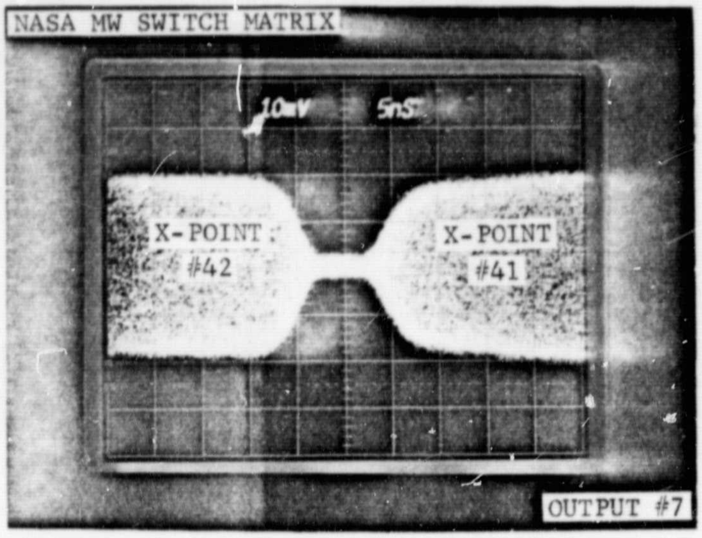
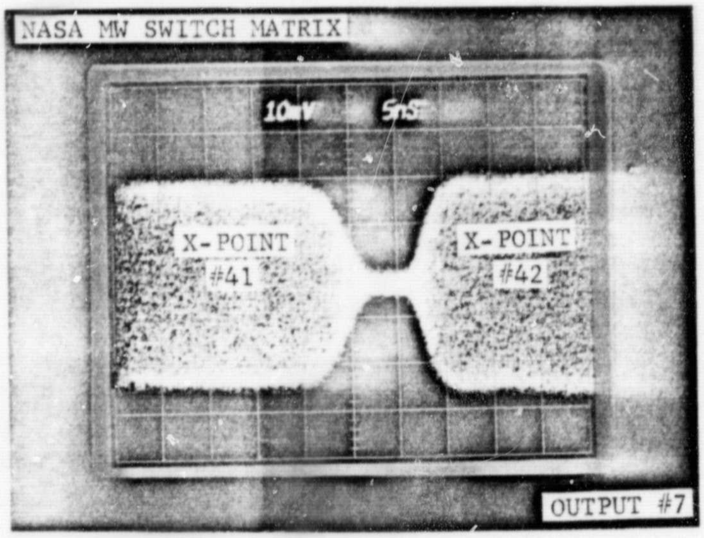


CROSSPOINTS #'s 41 AND 42
t = to #42 Switched "OFF"
#41 Switched "ON"



CROSSPOINTS #'s 41 AND 42
t = to #41 Switched "OFF"
#42 Switched "ON"

SWITCHING SPEED MEASUREMENT

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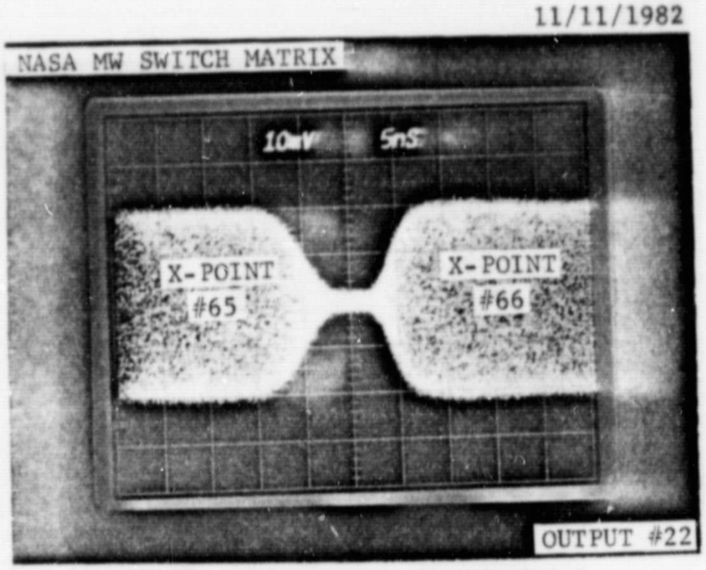
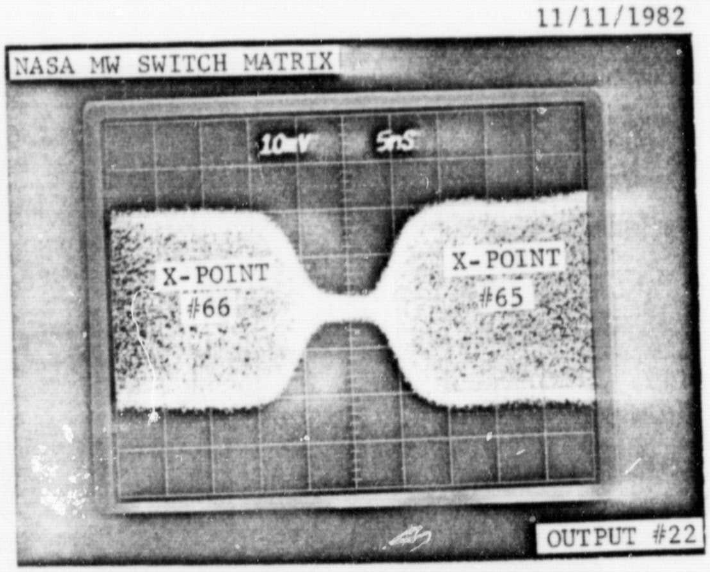


X-POINT #65 SWITCHED "OFF"
X-POINT #66 SWITCHED "ON"



X-POINT #66 SWITCHED "OFF"
X-POINT #65 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

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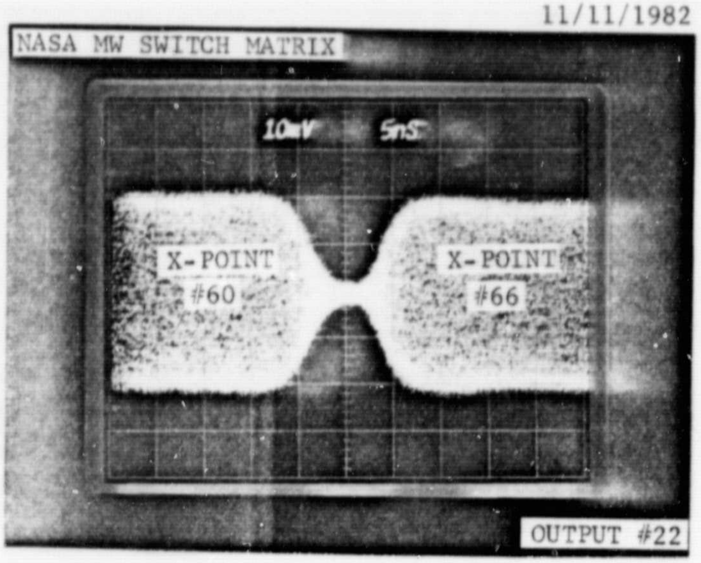
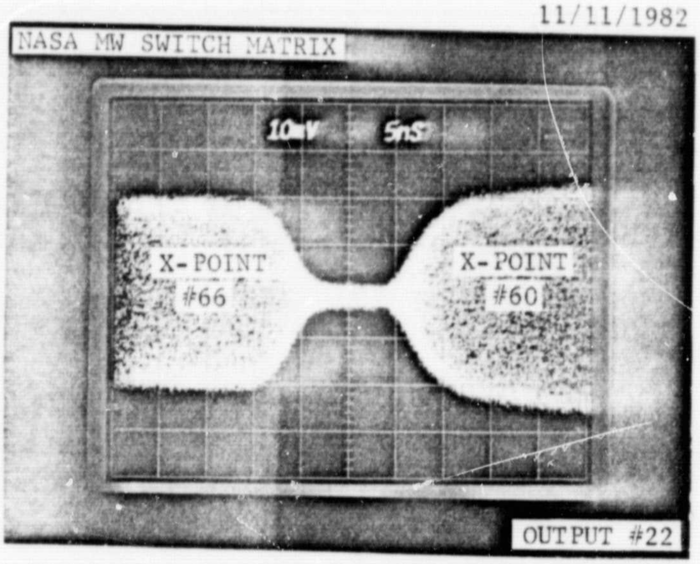


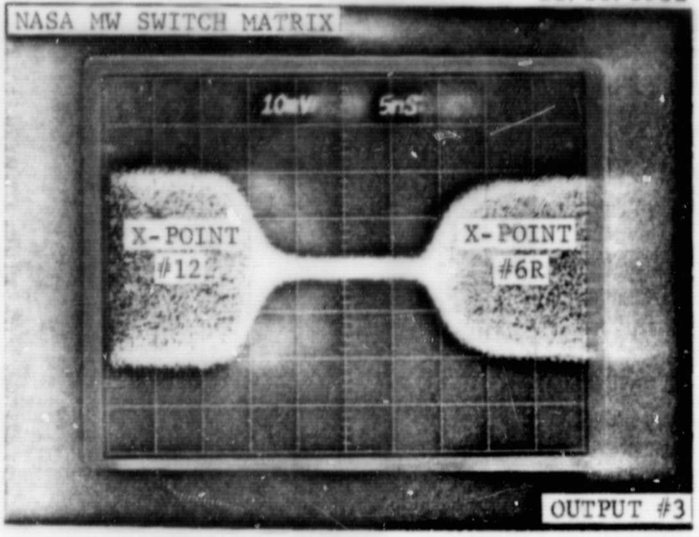
X-POINT #60 SWITCHED "OFF"
X-POINT #66 SWITCHED "ON"



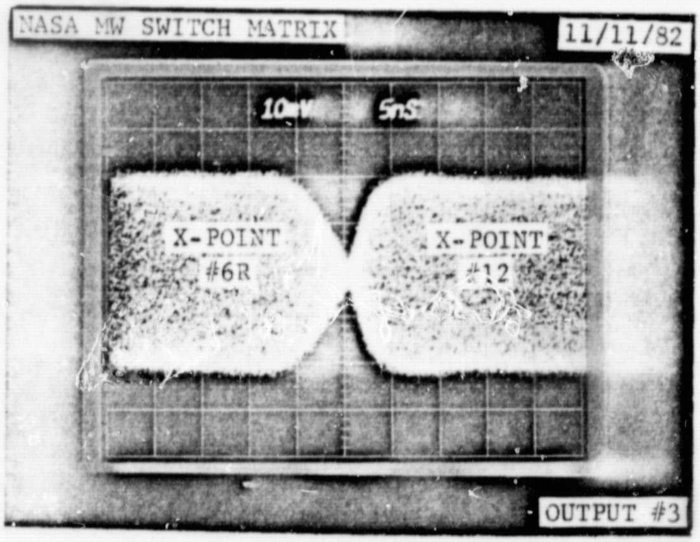
X-POINT #66 SWITCHED "OFF"
X-POINT #60 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

11/11/1982



X-POINT #12 SWITCHED "OFF"
X-POINT #6R SWITCHED "ON"



X-POINT #6R SWITCHED "OFF"
X-POINT #12 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

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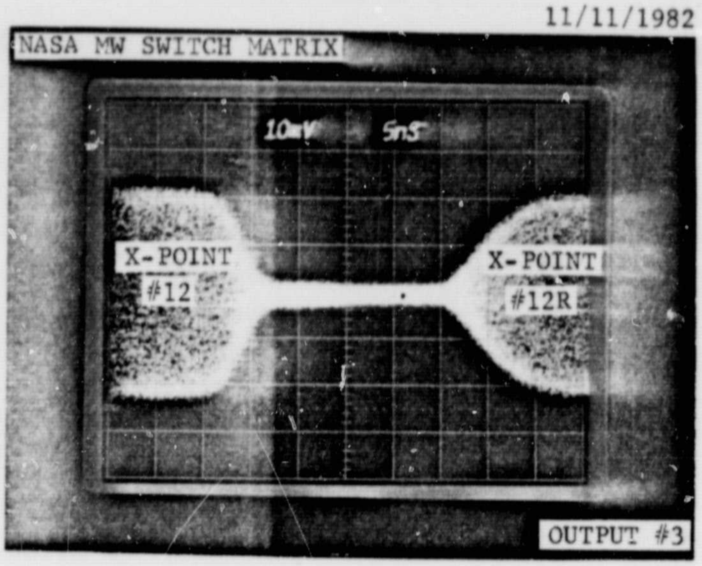
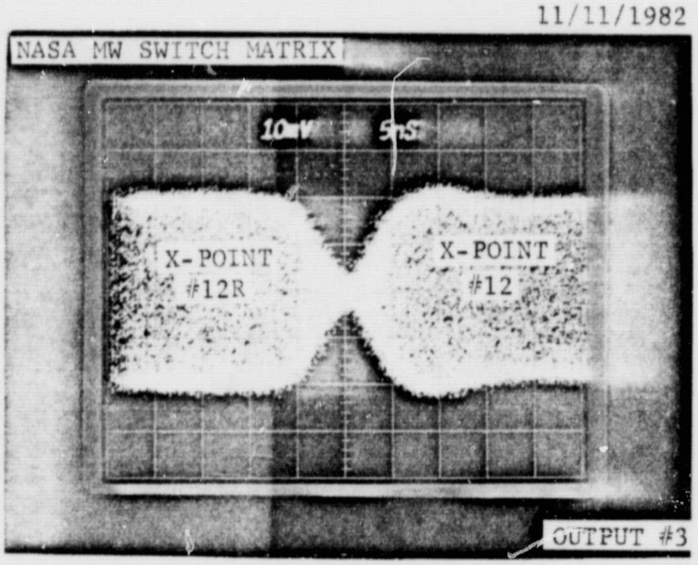


X-Point #12 SWITCHED "OFF"
X-POINT #12R SWITCHED "ON"



X-POINT #12R SWITCHED "OFF"
X-POINT #12 SWITCHED "ON"

SWITCHING SPEED MEASUREMENT

3.2.2

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #4

CONNECTIVITY TEST

Definition: Connectivity is defined as the capability of the matrix to connect any input port (#'s 3 thru 22) to any combination of 8 output ports (#'s 3, 4, 5, 6, 7, 13, 17 and 22) on a one-to-one basis. This qualitative test will check static and dynamic switching operation of all 66 active crosspoints of the matrix.

Test Setup: See Figure 3.2.2.1.

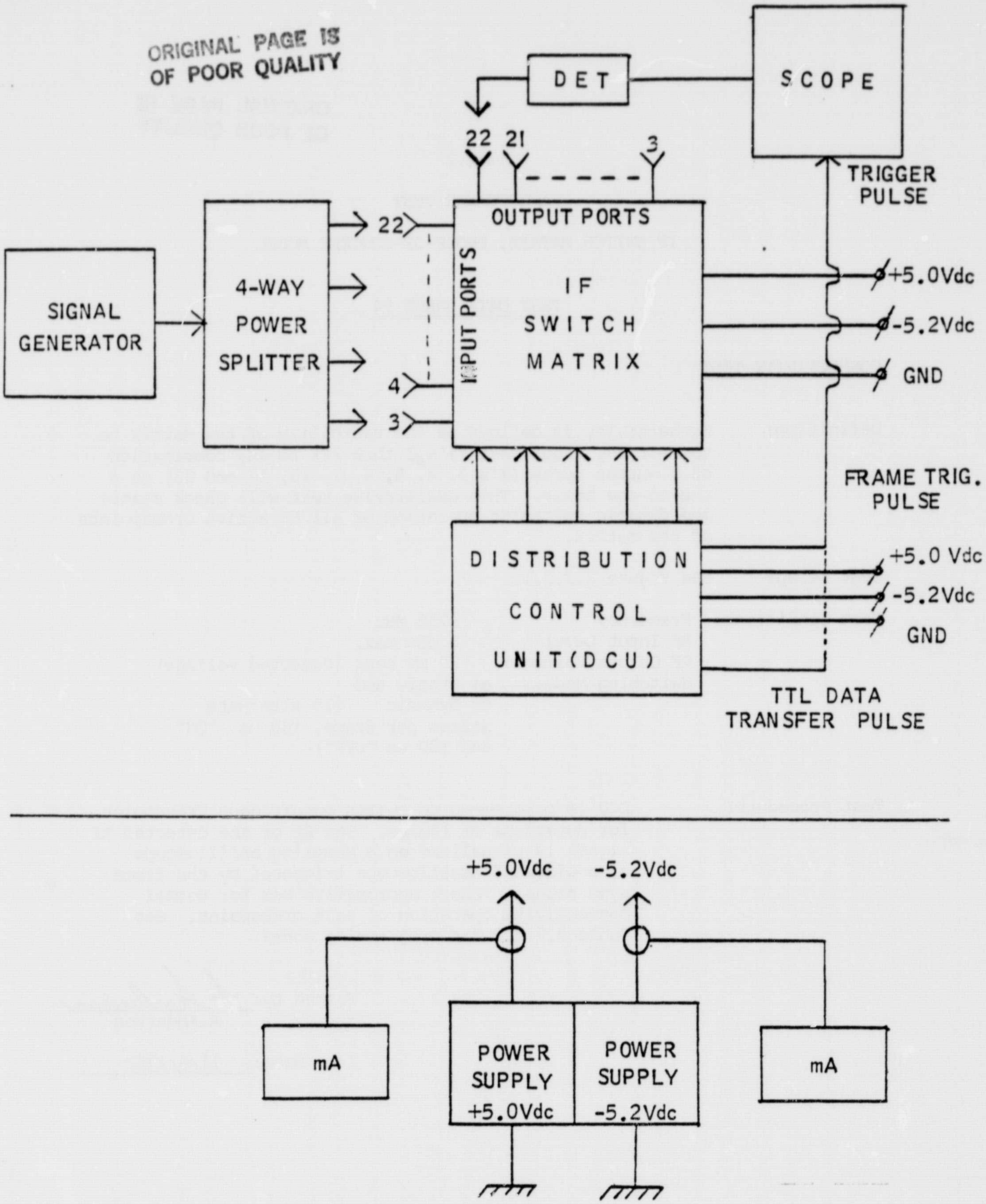
Test Conditions:

Frequency	4750 MHz
RF Input Level	0 dBm max.
RF Output Voltage:	20 mV peak (detected voltage)
Switching Mode:	a) Static and b) Dynamic (10 alternate states per frame, 100 us "ON" and 100 us "OFF")

Test Procedure: DCU is programmed to switch on-off each crosspoint for durations of 100 us. The RF or the detected RF signal is visualized on a sampling oscilloscope or a wideband oscilloscope triggered by the frame sync signal. Check appropriate box for normal connectivity operation of each crosspoint. See Table 3.2.2.1 for programming codes.

Tested by: A. Anderson
A.Anderson

Date: 11/5/1982



CONNECTIVITY TEST SET UP.

FIGURE 3.2.2.1

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CONNECTIVITY TEST DATA

Crosspoint #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Static	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Dynamic	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Crosspoint #	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
Static	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Dynamic	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Crosspoint #3	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66
Static	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Dynamic	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Tested by: A. Anderson
A.Anderson

Date: 11/5/1982

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TABLE 3.2.2.1

CROSSPOINT CODES for STATIC MODE OF OPERATION

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
X-Point 1	F	F	B	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 2	F	F	F	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 3	F	F	3	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 4	F	F	7	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 5	F	F	B	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 6	F	F	F	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 7	F	F	B	A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 8	F	F	F	A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 9	F	F	3	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 10	F	F	7	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 11	F	F	3	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 12	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 13	F	F	F	7	1	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 14	F	F	F	F	1	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 15	F	F	F	7	2	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 16	F	F	F	F	2	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 17	F	F	F	7	3	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 18	F	F	F	F	3	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 19	F	F	F	F	F	2	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 20	F	F	F	F	F	3	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0

CROSSPOINT CODES for STATIC MODE OF OPERATION

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
X-Point 21	F	F	F	F	F	4	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 22	F	F	F	F	F	5	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 23	F	F	F	F	F	6	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 24	F	F	F	F	F	7	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 25	F	F	F	F	F	F	5	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 26	F	F	F	F	F	F	7	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 27	F	F	F	F	F	F	9	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 28	F	F	F	F	F	F	B	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 29	F	F	F	F	F	F	D	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 30	F	F	F	F	F	F	F	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 31	F	F	F	F	F	F	F	B	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 32	F	F	F	F	F	F	F	F	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 33	F	F	F	F	F	F	F	3	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 34	F	F	F	F	F	F	F	7	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 35	F	F	F	F	F	F	F	B	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 36	F	F	F	F	F	F	F	F	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 37	F	F	F	F	F	F	F	B	A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 38	F	F	F	F	F	F	F	F	A	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 39	F	F	F	F	F	F	F	3	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 40	F	F	F	F	F	F	F	7	C	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0

ORIGINAL PAGE IS OF POOR QUALITY

CROSSPOINT CODES for STATIC MODE OF OPERATION

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
X-Point 41	F	F	F	F	F	F	F	3	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 42	F	F	F	F	F	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 43	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	E	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 44	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	7	E	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 45	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	A	E	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 46	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	B	E	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 47	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 48	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 49	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	4	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 50	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	5	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 51	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	6	E	F	F	F	F	F	F	0	0	0
X-Point 52	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	7	E	F	F	F	F	F	F	0	0	0
X-Point 53	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	A	E	F	F	F	F	F	F	0	0	0
X-Point 54	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	B	E	F	F	F	F	F	F	0	0	0
X-Point 55	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	F	F	F	F	F	F	F	0	0	0
X-Point 56	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	F	F	F	F	F	F	F	0	0	0
X-Point 57	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	4	F	F	F	F	F	F	F	0	0	0
X-Point 58	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	5	F	F	F	F	F	F	F	0	0	0
X-Point 59	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	D	C	0	0	0
X-Point 60	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	C	0	0	0

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OF POOR QUALITY

CROSSPOINT CODES for STATIC MODE OF OPERATION

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
X-Point 61	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	5	D	0	0	0
X-Point 62	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	7	D	0	0	0
X-Point 63	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	E	0	0	0
X-Point 64	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	3	E	0	0	0
X-Point 65	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	9	E	0	0	0
X-Point 66	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	B	E	0	0	0
X-Point 67	6	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 68	7	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 69	F	F	4	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 70	F	B	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 71	F	F	3	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 72	F	F	7	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
X-Point 73	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	E	F	F	F	F	F	F	0	0	0
X-Point 74	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	E	F	F	F	F	F	F	0	0	0
X-Point 75	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	C	0	0	0
X-Point 76	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	3	C	0	0	0

<u>STATE DURATION CODES</u> (Location 28,29 and 30)

Duration	Code	
1 uS	EFF	
2 uS	CFF	
4 uS	8FF	
5 uS	6FF	
6 uS	4FF	
10 uS	CEF	
20 uS	8DF	
43 uS	AAF	
50 uS	C9F	
60 uS	11F	
94 us	44F	
97 us	43F	
100 uS	83F	
150 uS	40E	
200 uS	07E	
300 uS	8AD	
400 uS	370	
500 uS	381	
999 uS	2FF	
1000 uS	0FF	
>>1000 uS	000	Static mode

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3.2.3

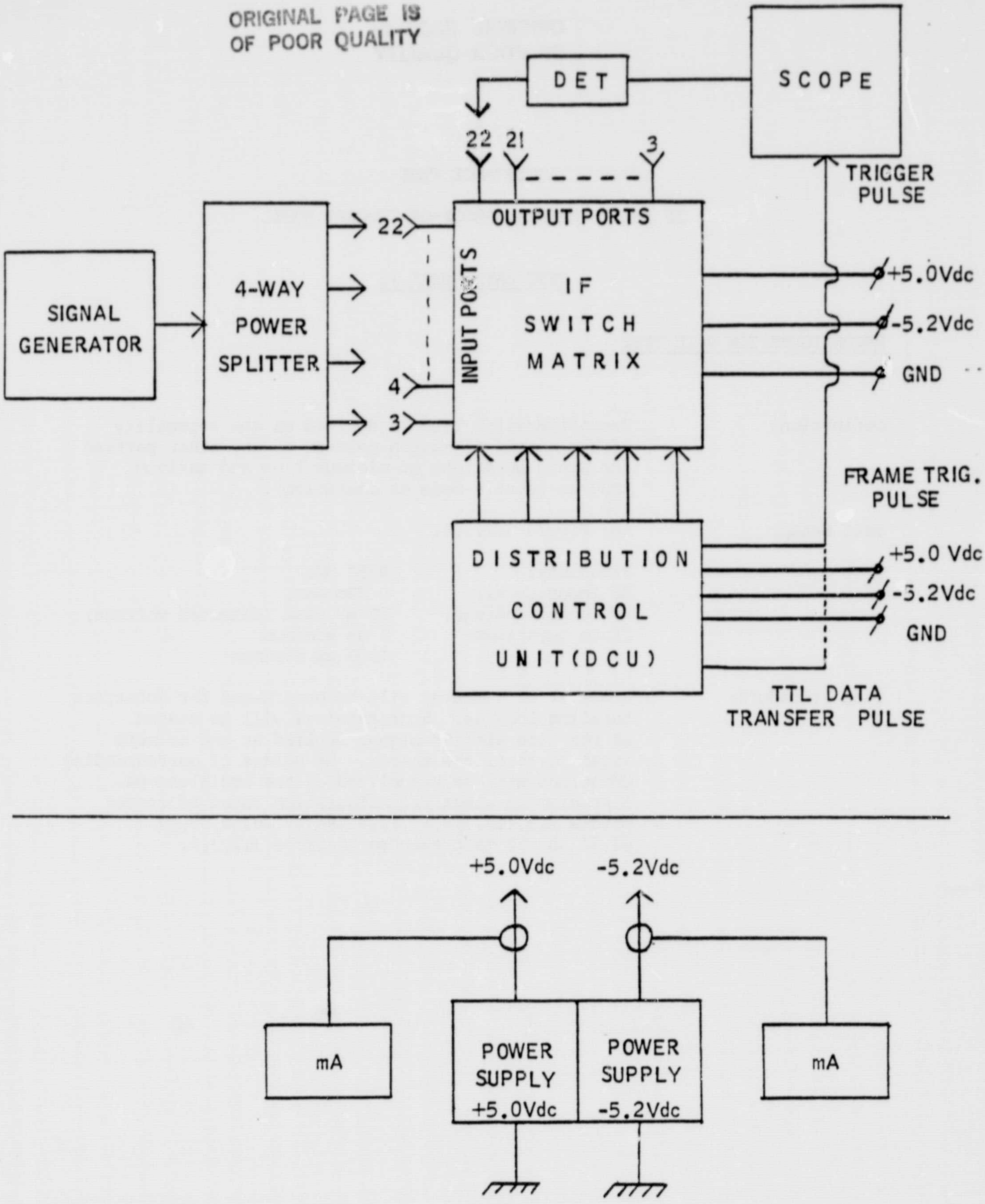
ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #5

RECONFIGURATION RATE TEST

Definition:	Reconfiguration rate is defined as the capability of the matrix to switch pattern to any other pattern for state durations of minimum 1 us and maximum 1000 us (static mode of operation).	
Test Setup:	See Figure 3.2.3.1.	
Test Conditions:	Frequency:	4750 MHz
	RF Input Level:	0 dBm max.
	RF Output Voltage:	20 mV peak (detected voltage)
	State Durations:	1 us minimum 1000 us maximum
Test Procedure:	A number of 8 states will be programmed for durations totaling 1000 us. 8 crosspoints will be tested at the time with RF signal applied at one or more input ports of the matrix. RF pulses of corresponding durations will be visualized on the oscilloscope. A program to check reconfiguration rates of crosspoints 1,3,4,5,6,8,10,12,43,44,46,48,50,59,60, 62,64 and 66 is presented in Table 3.2.3.1.	



Reconfiguration Test Set-Up

FIGURE 3.2.3.1

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TABLE 3.2.3.1

RECONFIGURATION RATE TEST DATA

State #	State Duration	X-Points ON	Check V	Comments
0	1 us	12,50,66	✓	
1	4 us	10,48,64	✓	
2	5 us	8,46,62	✓	
3	10 us	6,44,60	✓	
4	20 us	5,43,59	✓	
5	60 us	4,	✓	
6	100 us	3,	✓	
7	300 us	1,	✓	

Table 3.2.3.2 presents the programming code for this reconfiguration rate test.

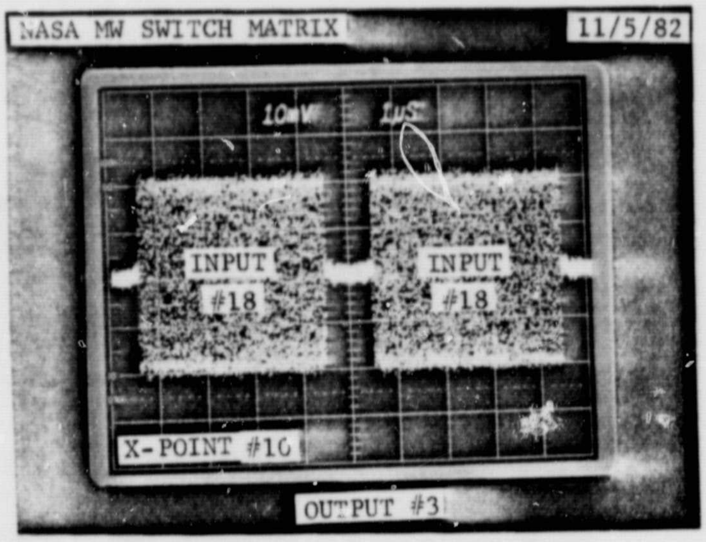
Tested by: A. Anderson
A.Anderson

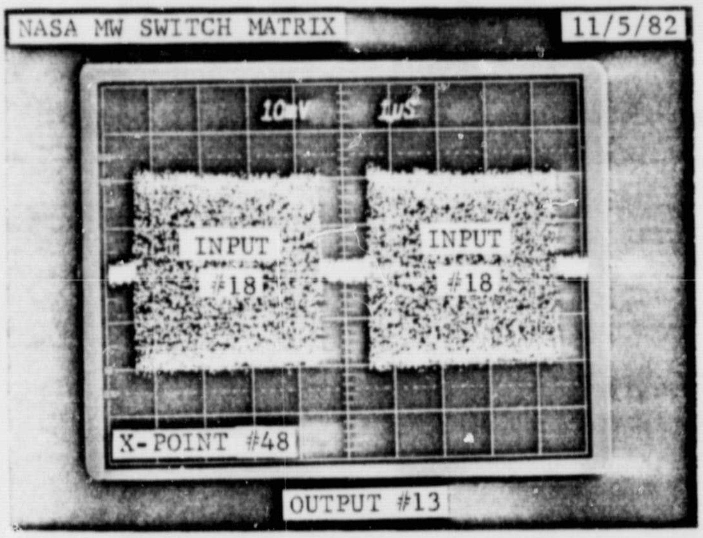
Date: 11/5/1982

TABLE 3.2.3.2

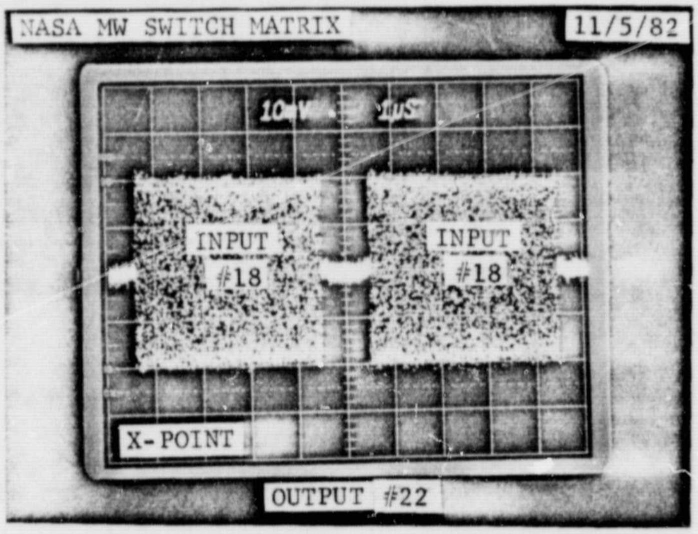
RECONFIGURATION RATE MEASUREMENT CODES (Example)

#'s ON	Sec	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
# 12,50,66	1µ	F	F	7	D	F	F	F	F	F	F	F	F	F	F	F	[illegible]	F	F	F	F	F	F	F	F	F	F	B	E	E	F	F
# 10,48,64	4µ	F	F	7	C	F	F	F	F	F	F	F	F	F	F	F	1	F	F	F	F	F	F	F	F	F	F	3	E	8	F	F
# 8,46 62	5µ	F	F	F	A	F	F	F	F	F	[illegible]	F	F	F	F	F	B	E	F	F	F	F	F	F	F	F	F	7	D	6	F	F
# 6,44,60	10µ	F	F	F	9	F	F	F	F	F	F	F	F	F	F	F	7	E	F	F	F	F	F	F	F	F	F	F	C	C	E	F
# 5 43 59	20µ	F	F	B	9	F	F	F	F	F	F	F	F	F	F	F	6	E	F	F	F	F	F	F	F	F	F	D	C	8	D	F
# 4	60µ	F	F	7	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	8	8	F
# 3	100µ	F	F	3	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	8	3	F
# 1	300µ	F	F	B	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	9	A	D
All X-Points 0=c		F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0





STATE DURATION
1 μs "ON"
4 μs "OFF



RECONFIGURATION RATE MEASUREMENT

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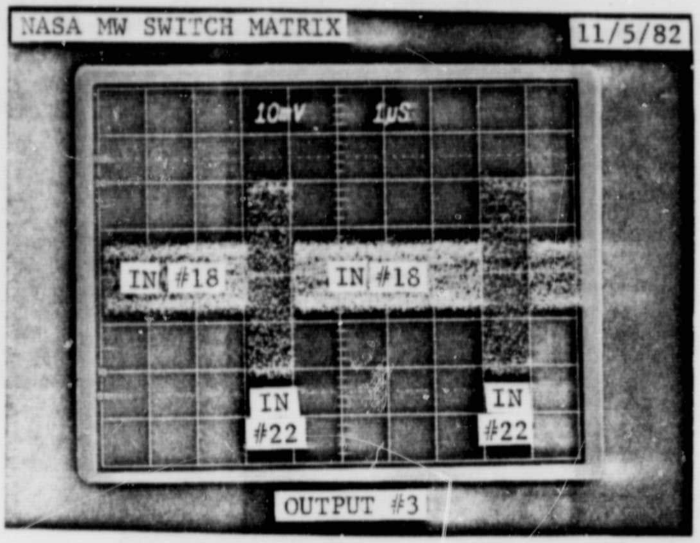
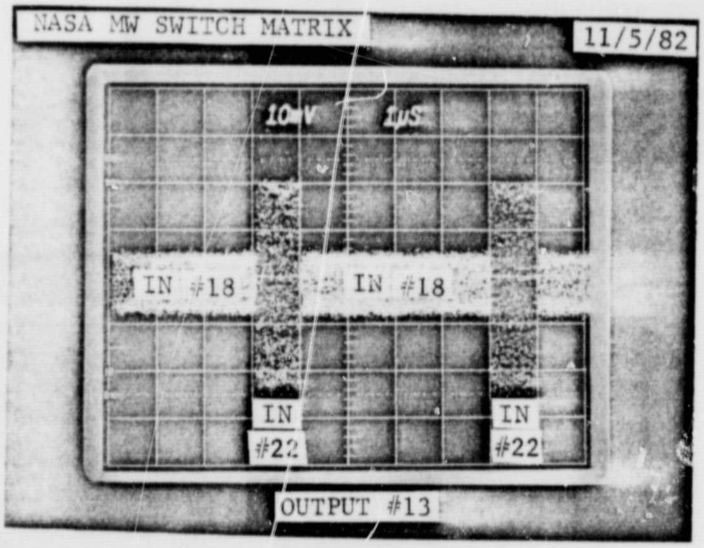


Reconfigure from crosspoint #10 to Crosspoint #12



Reconfigure from crosspoint #48 to Crosspoint #50

NOTE: Input power levels are not equal at Ports 18 and 22.

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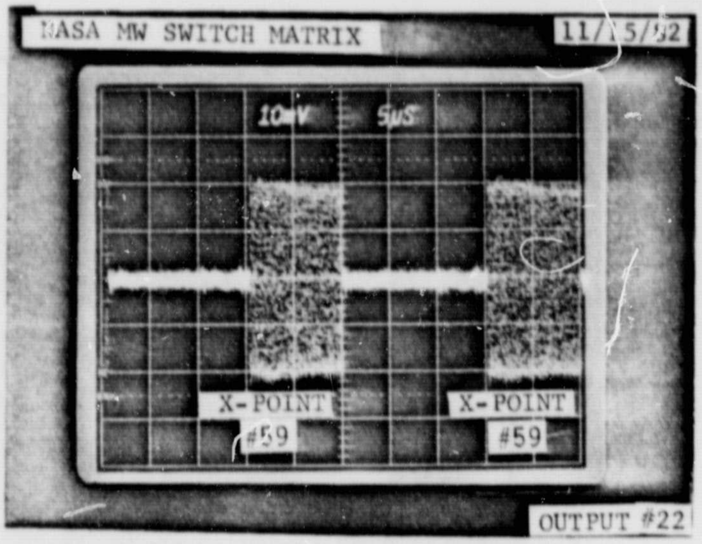
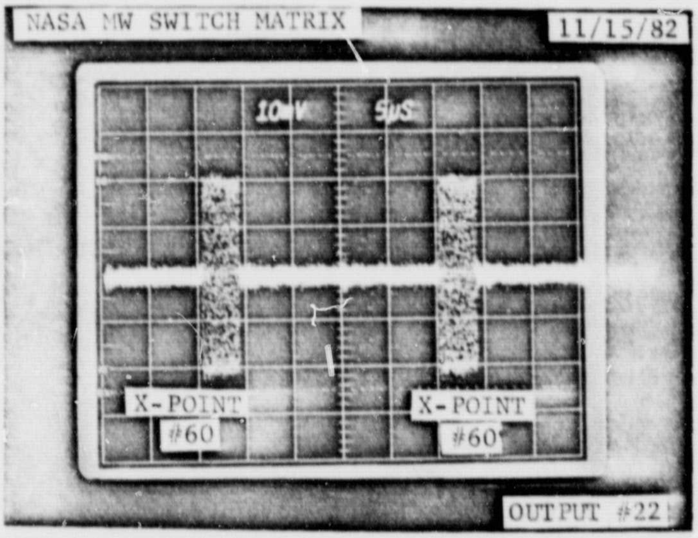


STATE DURATION
10 μs "ON"
15 μs "OFF"



STATE DURATION
4 μs "ON"
21 μs "OFF"

RECONFIGURATION RATE MEASUREMENT

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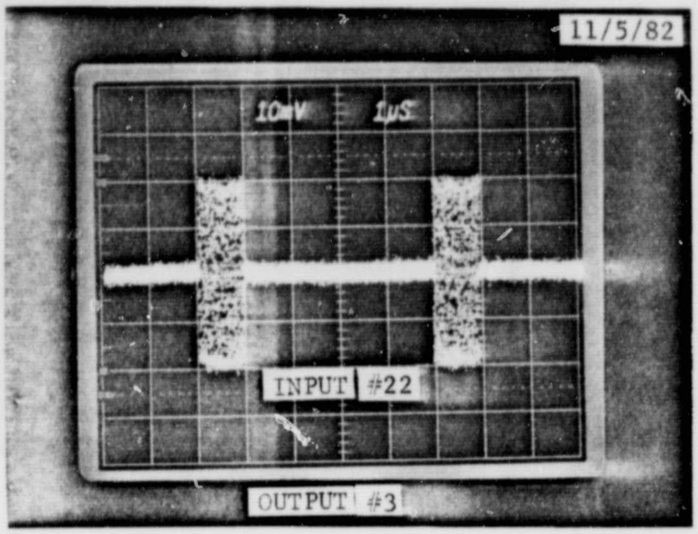

STATE DURATION
1 μs "ON"
4 μs "OFF"

RECONFIGURATION RATE MEASUREMENT

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3.2.4

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #6

BROADCAST MODE OF OPERATION TEST

Definition:	Broadcast mode of operation is defined as system capability of connecting any input signal to all output ports of the matrix.
Test Setup:	See Figure 3.2.4.1.
Test Conditions:	Frequency: 4750 MHz RF Input Level: 0 dBm max. RF Output Level: 20 mV peak Switching mode: Dynamic, state duration 100 us minimum
Test Procedure:	With the RF signal applied at one or more input ports of the matrix, the output signal is identified on the scope screen . The codes to test the broadcast mode for each input port are presented in Table 3.2.4.1. The duration code is selected from Table 3.2.4.2 The test was performed for "ON" state durations of 200 us and alternate "OFF" states of 50 us. See attached photos.

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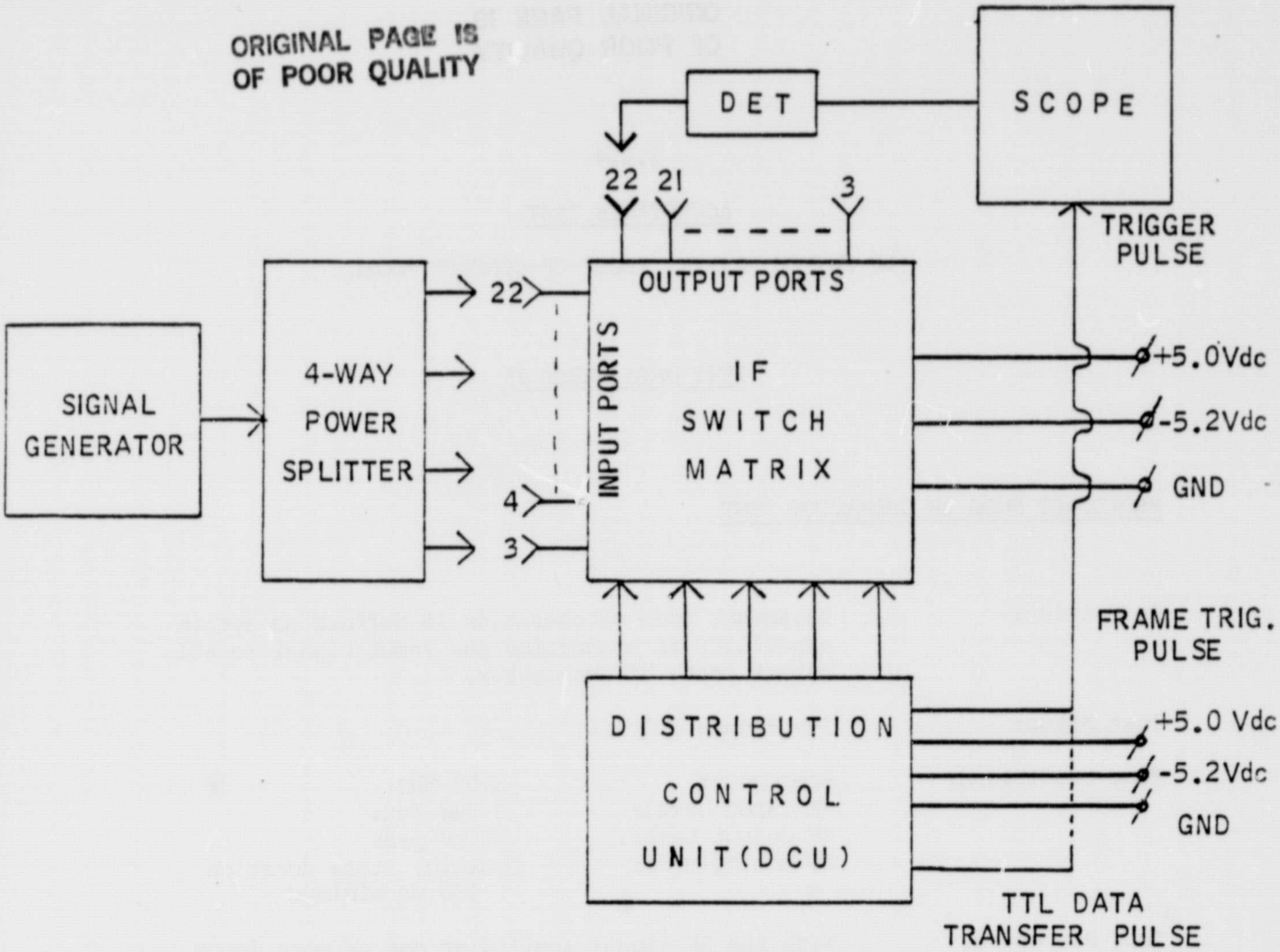

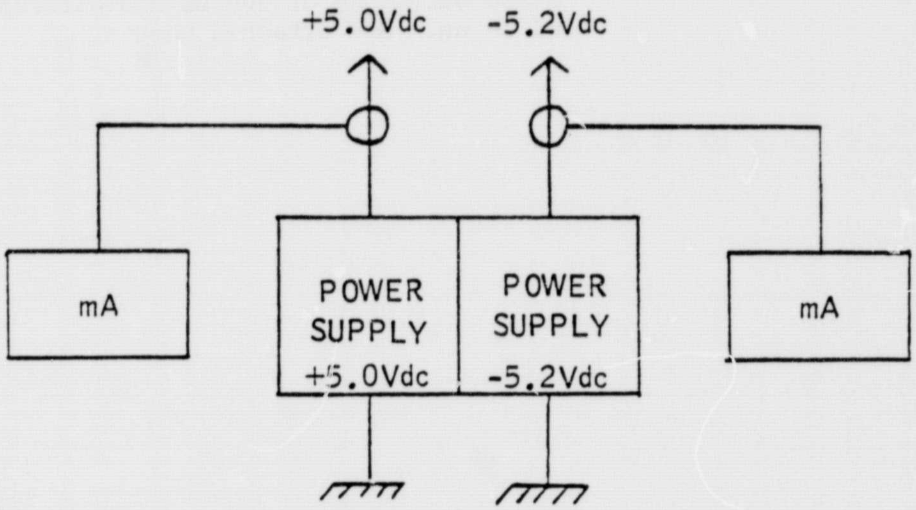

BROADCAST MODE TEST SET-UP

FIGURE 3.2.4.1

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TABLE 3.2.4.1

BROADCAST MODE TEST DATA

Input Port	Crosspoint #'s	Output Ports	Check √
3	1,13,19,25,31	3,4,5,6,7	✓
4	2,14,20,26,32	3,4,5,6,7	✓
5	3,15,21,27,33	3,4,5,6,7	✓
6	4,16,22,28,34	3,4,5,6,7	✓
7	5,17,23,29,35,43,51,59	3,4,5,6,7,13,17,22	✓
8	6,18,24,30,36,44,52,60	3,4,5,6,7,13,17,22	✓
11	7,37,45,53,61	3,7,13,17,22	✓
12	8,38,46,54,62	3,7,13,17,22	✓
17	9,39,47,55,63	3,7,13,17,22	✓
18	10,40,48,56,64	3,7,13,17,22	✓
21	11,41,49,57,65	3,7,13,17,22	✓
22	12,42,50,58,66	3,7,13,17,22	✓

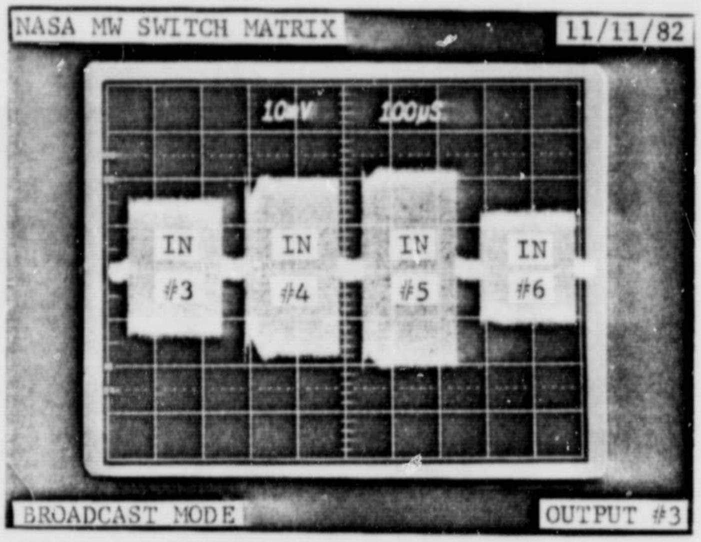
Tested by: A. Anderson
A. Anderson

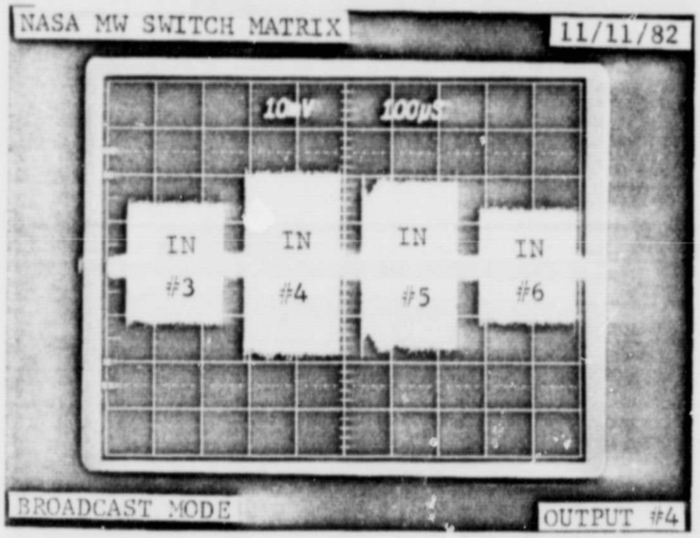
Date: 11/11/1982

TABLE 3.2.4.2

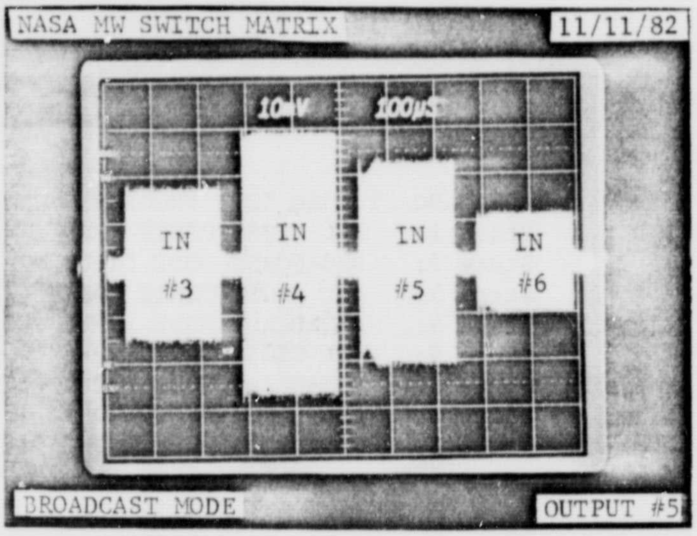
PROGRAMMING CODES FOR BROADCAST MODE OF OPERATION

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Broadcast #3	F	F	B	0	1	2	4	8	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
Broadcast #4	F	F	F	8	1	3	6	C	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
Broadcast #5	F	F	3	1	2	4	8	0	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
Broadcast #6	F	F	7	9	2	5	A	4	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
Broadcast #7	F	F	B	1	3	6	C	8	9	F	F	F	F	F	F	6	E	F	F	F	6	E	F	F	F	F	D	C	0	0	0
Broadcast #8	F	F	F	9	3	7	E	C	9	F	F	F	F	F	F	7	E	F	F	F	7	E	F	F	F	F	F	C	0	0	0
Broadcast #11	F	F	B	A	F	F	F	B	A	F	F	F	F	F	F	A	E	F	F	F	A	E	F	F	F	F	5	D	0	0	0
Broadcast #12	F	F	F	A	F	F	F	F	A	F	F	F	F	F	F	B	E	F	F	F	B	E	F	F	F	F	7	D	0	0	0
Broadcast #17	F	F	3	C	F	F	F	3	C	F	F	F	F	F	F	0	F	F	F	F	0	F	F	F	F	F	1	E	0	0	0
Broadcast #18	F	F	7	C	F	F	F	7	C	F	F	F	F	F	F	1	F	F	F	F	1	F	F	F	F	F	3	E	0	0	0
Broadcast #21	F	F	3	D	F	F	F	3	D	F	F	F	F	F	F	4	F	F	F	F	4	F	F	F	F	F	9	E	0	0	0
Broadcast #22	F	F	7	D	F	F	F	7	D	F	F	F	F	F	F	5	F	F	F	F	5	F	F	F	F	F	B	E	0	0	0





BROADCAST
MODE



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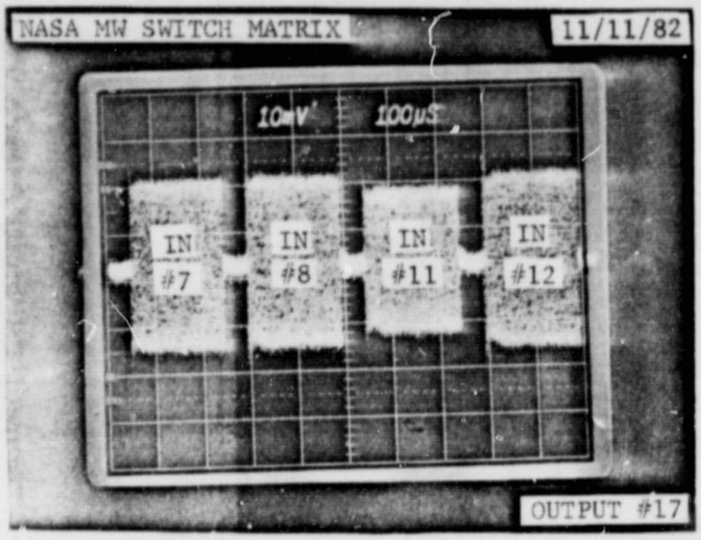

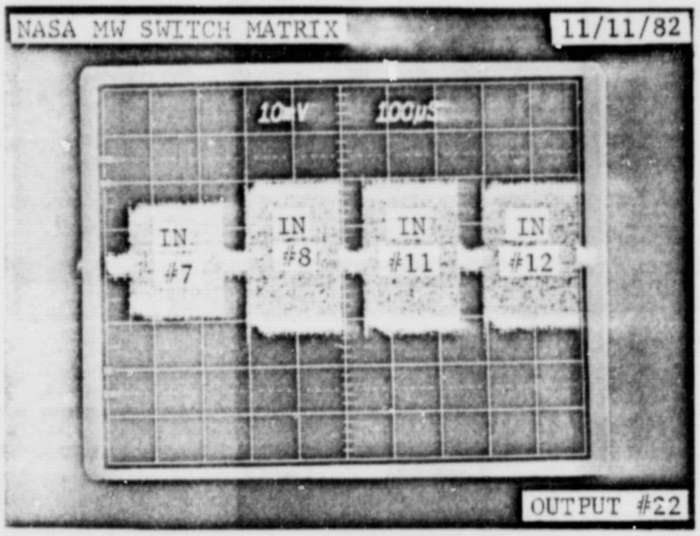

BROADCAST MODE TEST PROGRAM

State 1:	ALL CROSSPOINTS "OFF"	50 µs
State 2:	BROADCAST MODE INPUT #7	200 µs
State 3:	ALL CROSSPOINTS "OFF"	50 µs
State 4:	BROADCAST MODE INPUT #8	200 µs
State 5:	ALL CROSSPOINTS "OFF"	50 µs
State 6:	BROADCAST MODE INPUT #11	200 µs
State 7:	ALL CROSSPOINTS "OFF"	50 µs
State 8:	BROADCAST MODE INPUT #12	200 µs
	TOTAL	1000 µs

3.2.5

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #7

REDUNDANT (WRAPAROUND) MODE OF OPERATION TEST

Definition:	Capability of rerouting the input signal using a wraparound path.	
Test Setup:	See Figure 3.2.5.1.	
Test Conditions:	Frequency:	4750 MHz
	RF Input Level:	Max. 0 dBm
	Switching Mode:	Static and dynamic, 100 us state duration.
Test Procedure:	Measure and record on data sheet the insertion loss in the static mode of operation (duration code "000") and then check dynamic mode of operation of each of the crosspoints provided with redundant paths. See Table 3.2.5.1 for the DCU programming code for redundant paths. Use duration code "83F" for 100 us state duration in the dynamic mode.	

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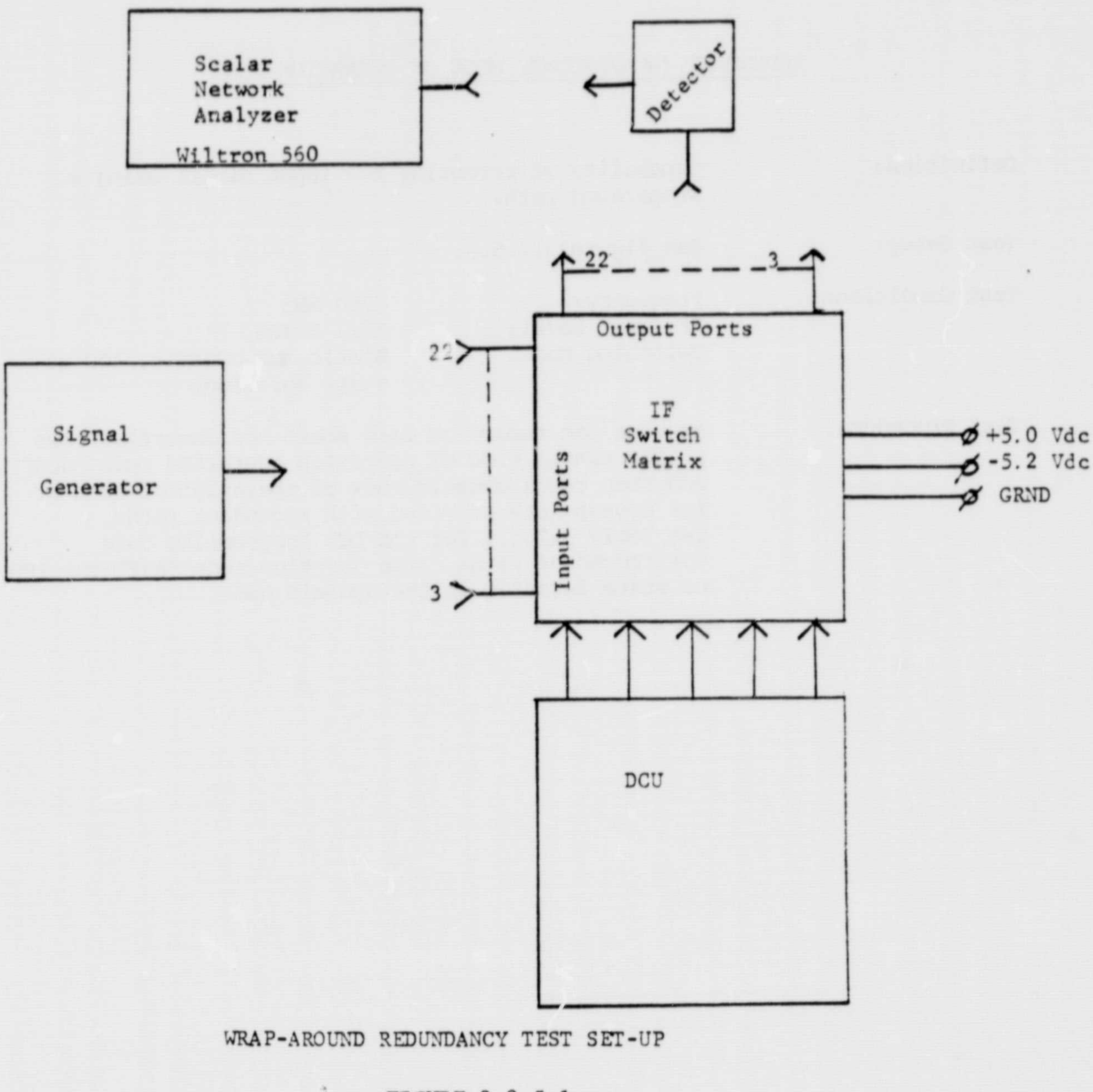

WRAP-AROUND REDUNDANCY TEST SET-UP

FIGURE 3.2.5.1

REDUNDANT CROSSPOINT OPERATION TEST DATA

Crosspoint #	Redundant Path	Insertion Loss, static	Dynamic mode (v)	Comments
5R	67 + 71	25.0 dB	✓	*See Note
6R	68 + 71	25.0 dB	✓	*See Note
11R	69 + 72	20.0 dB	✓	
12R	70 + 72	20.0 dB	✓	
51R	67 + 73	22.0 dB	✓	
52R	68 + 73	22.0 dB	✓	
57R	69 + 74	15.0 dB	✓	
58R	70 + 74	16.0 dB	✓	
59R	67 + 75	21.0 dB	✓	
60R	68 + 75	21.0 dB	✓	
65R	69 + 76	16.0 dB	✓	
66R	70 + 76	17.0 dB	✓	

* Note: Higher insertion loss due to a cummulative effect of lower gain of switch amplifier modules for crosspoints #'s 67+68 and 71+72 at center frequency.

Tested by: A. Anderson
A. Anderson

Date: 11/10/1982

TABLE 3.2.5.1

DCU Programming Code for Redundant Signal Paths.

CROSSPOINT CODES (Redundant Path)

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
#5R (67+71)	6	E	3	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
#6R (68+71)	7	E	3	9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
#11R (69+72)	F	9	6	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
#12R (70+72)	F	B	6	8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0
#51R (67+73)	6	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	E	F	F	F	F	F	F	0	0	0
#52R (68+73)	7	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	E	F	F	F	F	F	F	0	0	0
#57R (69+74)	F	F	4	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	E	F	F	F	F	F	F	0	0	0
#58R (70+74)	F	F	5	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	E	F	F	F	F	F	F	0	0	0
#59R (67+75)	6	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	C	0	0	0
#60R (68+75)	7	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	1	C	0	0	0
#65R (69+76)	F	F	4	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	3	C	0	0	0
#66R (70+76)	F	F	5	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	3	C	0	0	0
ALL OFF	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	0	0	0

3.3 Frequency Domain Tests

To accurately characterize the passband and linearity characteristics, several tests were performed. The tests included several semi-automatic and manual tests (this section) as well as a complete set of Automatic Network Analyzer tests detailed in Section 3.5. The semi-automatic system tested "ON" and "OFF" gain as well as power out, phase shift, and DC power consumption with respect to input power. Output VSWR for a sample of crosspoints was measured using a scalar network analyzer system. The thermal vacuum system test also used a semi-automatic system with before and after response curves taken on a scalar network analyzer system. Temperature compensation on a single switch amplifier was also performed using a manual set-up and scalar network analyzer.

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3.3.1

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #8

SEMI-AUTOMATIC ELECTRICAL TESTS

Defintion: The semi-automatic electrical tests will measure and plot the following electrical parameters of selected crosspoints of the matrix:

a. Insertion Loss versus frequency in "ON" state
b. Reverse Isolation vs frequency in the "OFF" state
c. Output Power versus Input Power (1-dB compression)
d. Phase versus input power
e. Power consumption and DC current versus input power

Test Setup: See Figure 3.3.1.1.

Test Conditions:	Frequency:	3.5 Ghz to 6.0 Ghz for (a) and (b) 4.75 Ghz for (c), (d) and (e)
	Input Power:	Nominal: -10 dBm Maximum: +18 dBm

Test Procedures: See Instructions Manual

Test Data: For crosspoint #'s 6, 31, 37 and 66. Attach computer printouts and plots.*
Note: 1-dB compression point is higher than +16 dBm for all crosspoints of the matrix (RF input power).

Tested by: A. Anderson
A.Anderson

Date: 11/4/1982

* Additional test data is also presented for crosspoints #'s 16, 23, and 45. See attached data sheets.

NASA SWITCH MODULE TEST SET-UP

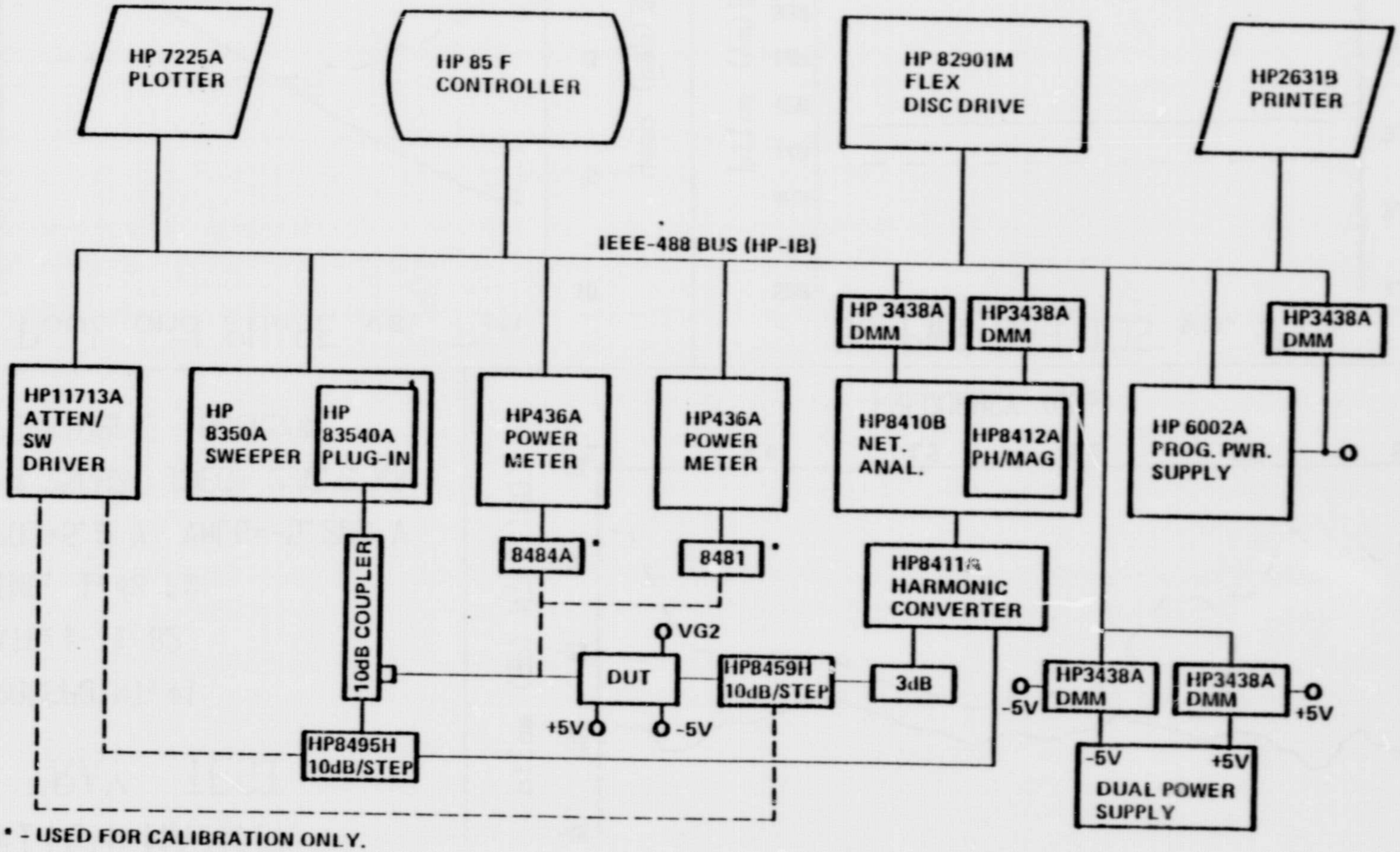

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FIGURE 3.3.1.1

SWITCH MATRIX
TRAY TEST

CROSSPOINT: #1

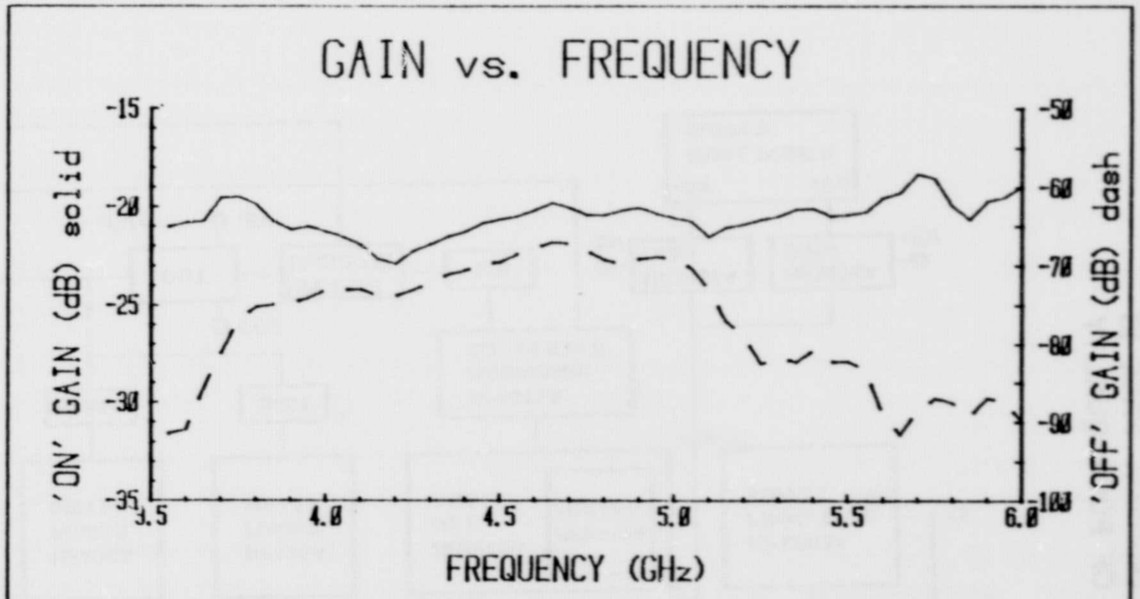
DATE: 1-11-82

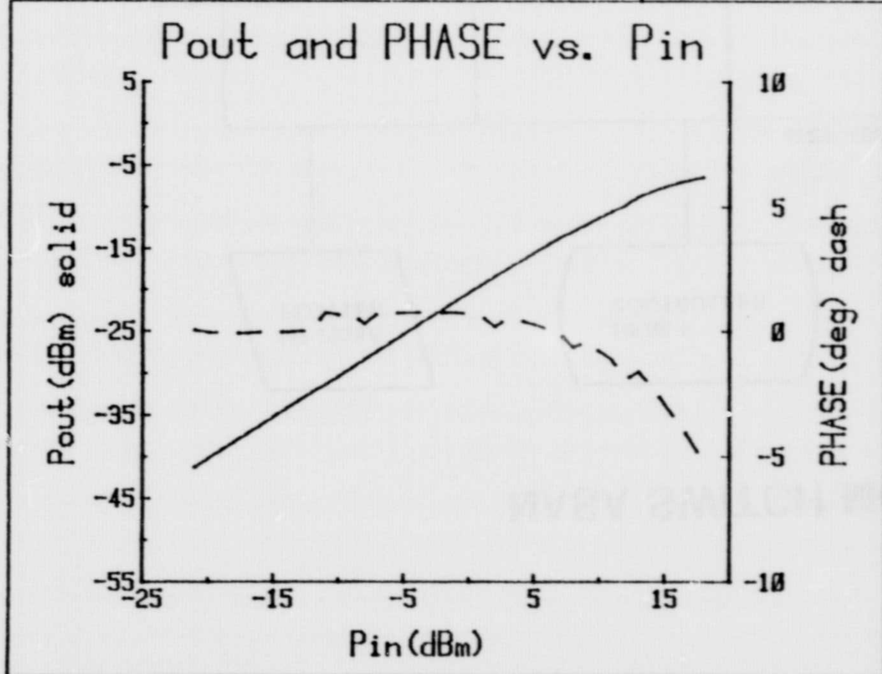
TIME: 1:48 PM

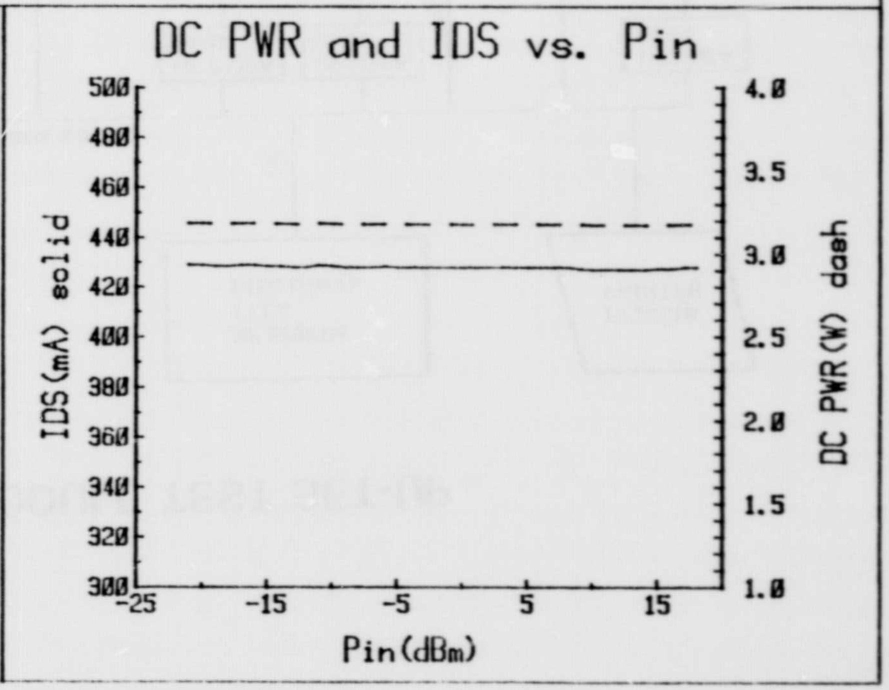
VPOS=5.Ø V VNEG=-5.2ØØ V

F=4.75GHZ INEG= 2ØØ.Ø mA

OPERATOR: A. ANDERSON







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SWITCH MATRIX TRAY TEST

CROSSPOINT: #1 DATE: 1-11-82 TIME: 1:48 PM

VPOS= 5.00 V VNEG=-5.20 V INEG= 200.0 mA OPERATOR:A. ANDERSON

SWEPT FREQUENCY DATA			SWEPT POWER DATA			F=4.75 GHz.	
FREQ (MHz)	ON GAIN (dB)	OFF GAIN (dB)	Pin (dBm)	Pout (dBm)	PHASE (deg)	DC PWR (W)	IDS (mA)
3500	-21.08	-91.16	-22.00	-42.30	0.0	3.18	428.5
3550	-21.03	-91.50	-21.00	-41.27	.0	3.19	429.0
3600	-20.81	-90.92	-20.00	-40.24	-.1	3.19	429.0
3650	-20.74	-85.72	-19.00	-39.24	-.1	3.18	428.5
3700	-19.54	-81.15	-18.00	-38.24	-.1	3.18	428.5
3750	-19.49	-76.79	-17.00	-37.24	-.1	3.19	429.0
3800	-19.87	-75.23	-16.00	-36.24	-.1	3.19	429.0
3850	-20.74	-74.87	-15.00	-35.25	-.1	3.18	428.5
3900	-21.17	-74.74	-14.00	-34.24	-.1	3.18	428.5
3950	-21.02	-74.03	-13.00	-33.24	0.0	3.18	428.0
4000	-21.27	-73.03	-12.00	-32.24	.0	3.18	428.0
4050	-21.54	-73.04	-11.00	-31.36	.7	3.19	429.0
4100	-21.94	-72.94	-10.00	-30.37	.7	3.18	428.5
4150	-22.66	-73.82	-9.00	-29.37	.7	3.18	428.0
4200	-22.91	-73.78	-8.00	-28.37	.3	3.18	428.0
4250	-22.26	-73.05	-7.00	-27.38	.7	3.18	428.0
4300	-21.92	-72.15	-6.00	-26.39	.7	3.18	428.5
4350	-21.53	-71.11	-5.00	-25.39	.7	3.18	428.0
4400	-21.28	-70.60	-4.00	-24.39	.7	3.18	428.0
4450	-20.85	-69.75	-3.00	-23.40	.8	3.18	428.0
4500	-20.64	-69.54	-2.00	-22.41	.7	3.18	428.0
4550	-20.48	-68.52	-1.00	-21.37	.7	3.18	428.0
4600	-20.19	-67.78	0.00	-20.39	.7	3.18	428.0
4650	-19.80	-67.03	1.00	-19.41	.6	3.18	428.0
4700	-20.06	-67.24	2.00	-18.44	.2	3.18	428.0
4750	-20.43	-68.17	3.00	-17.43	.5	3.18	428.0
4800	-20.42	-69.28	4.00	-16.47	.4	3.18	428.0
4850	-20.19	-69.80	5.00	-15.51	.3	3.18	428.0
4900	-20.04	-69.14	6.00	-14.59	.1	3.18	428.0
4950	-20.37	-68.86	7.00	-13.67	-.1	3.18	428.0
5000	-20.58	-69.13	8.00	-12.91	-.6	3.18	428.0
5050	-20.75	-70.29	9.00	-12.12	-.4	3.18	427.5
5100	-21.53	-72.90	10.00	-11.29	-.8	3.18	427.0
5150	-21.06	-77.02	11.00	-10.51	-1.1	3.18	427.0
5200	-20.90	-78.86	12.00	-9.79	-1.9	3.18	427.0
5250	-20.67	-82.52	13.00	-8.76	-1.6	3.18	427.0
5300	-20.49	-81.68	14.00	-8.15	-2.2	3.18	427.0
5350	-20.13	-82.31	15.00	-7.61	-2.9	3.18	427.5
5400	-20.10	-80.77	16.00	-7.14	-3.6	3.18	427.5
5450	-20.50	-82.25	17.00	-6.74	-4.3	3.18	428.0
5500	-20.40	-82.19	18.00	-6.42	-5.2	3.18	428.0
5550	-20.27	-83.35	0.00	0.00	0.0	0.00	0.0
5600	-19.55	-88.84	0.00	0.00	0.0	0.00	0.0
5650	-19.28	-91.55	0.00	0.00	0.0	0.00	0.0
5700	-18.31	-88.51	0.00	0.00	0.0	0.00	0.0
5750	-18.56	-86.96	0.00	0.00	0.0	0.00	0.0
5800	-19.95	-87.55	0.00	0.00	0.0	0.00	0.0
5850	-20.64	-89.22	0.00	0.00	0.0	0.00	0.0
5900	-19.70	-86.97	0.00	0.00	0.0	0.00	0.0
5950	-19.50	-87.29	0.00	0.00	0.0	0.00	0.0
6000	-18.95	-89.90	0.00	0.00	0.0	0.00	0.0

SWITCH MATRIX
TRAY TEST

CROSSPOINT: #6

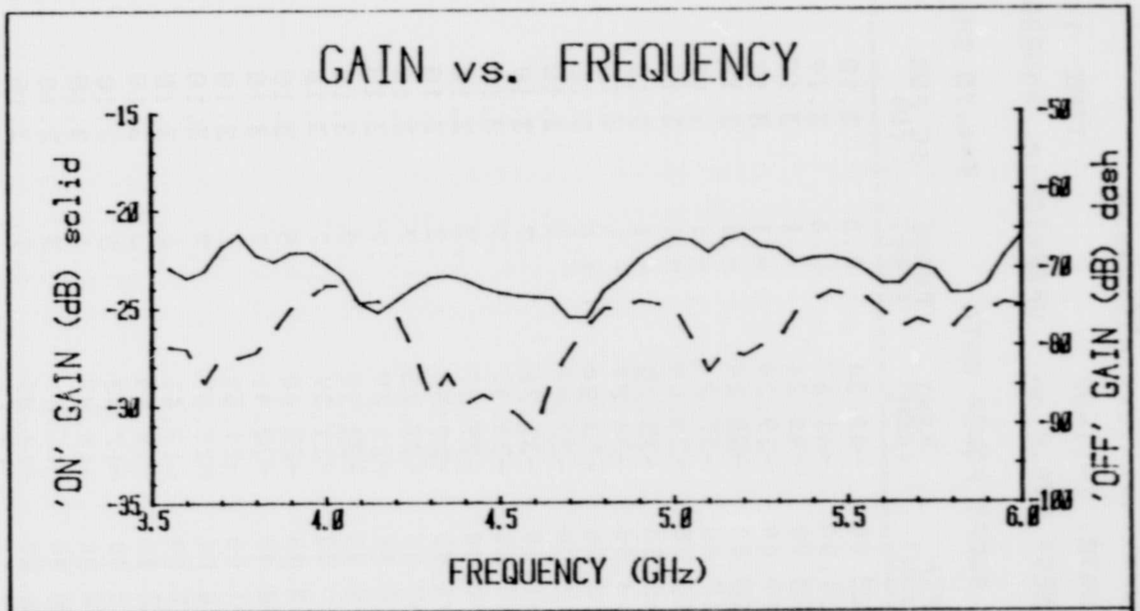
DATE: 1-11-82

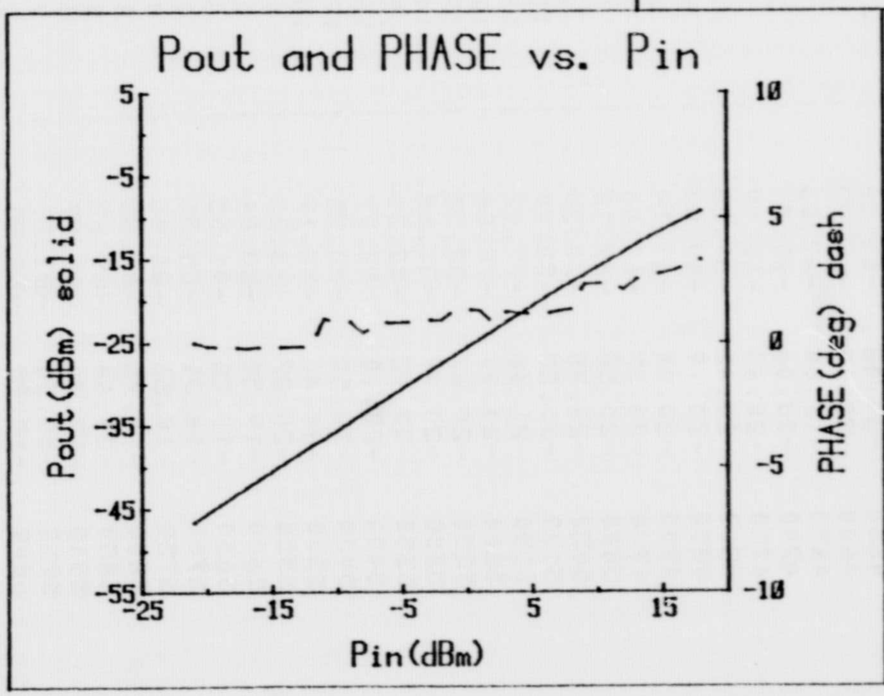
TIME: 2:24 PM

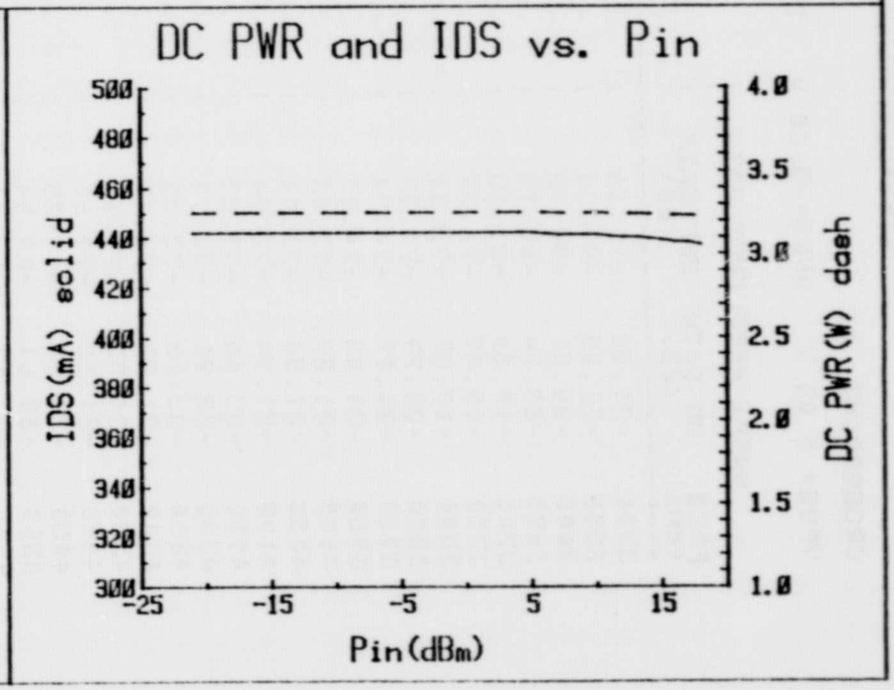
VPOS=5.0 V VNEG=-5.210 V

F=4.75GHZ INEG= 200.0 mA

OPERATOR: A. ANDERSON







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SWITCH MATRIX TRAY TEST

CROSSPOINT: #6 DATE: 1-11-82 TIME: 2:24 PM

VPOS= 5.00 V VNEG=-5.21 V INEG= 200.0 mA OPERATOR:A. ANDERSON

SWEPT FREQUENCY DATA			SWEPT POWER DATA			F=4.75 GHz.	
FREQ (MHz)	ON GAIN (dB)	OFF GAIN (dB)	Pin (dBm)	Pout (dBm)	PHASE (deg)	DC PWR (W)	IDS (mA)
3500	-22.75	-79.35	-22.00	-47.59	0.0	3.25	442.0
3550	-22.91	-79.99	-21.00	-46.56	-.0	3.25	442.0
3600	-23.43	-80.32	-20.00	-45.53	-.2	3.25	442.0
3650	-23.04	-84.51	-19.00	-44.53	-.2	3.25	442.0
3700	-21.86	-81.18	-18.00	-43.52	-.2	3.25	442.0
3750	-21.23	-81.36	-17.00	-42.51	-.2	3.25	442.0
3800	-22.26	-80.66	-16.00	-41.51	-.2	3.25	442.0
3850	-22.59	-77.99	-15.00	-40.51	-.2	3.25	442.0
3900	-22.13	-74.95	-14.00	-39.50	-.2	3.25	442.0
3950	-22.13	-73.57	-13.00	-38.50	-.2	3.25	442.0
4000	-22.68	-72.05	-12.00	-37.49	-.2	3.25	442.0
4050	-23.36	-72.09	-11.00	-36.64	1.0	3.25	442.0
4100	-24.79	-74.32	-10.00	-35.63	.8	3.25	442.0
4150	-25.24	-74.05	-9.00	-34.63	.8	3.25	442.0
4200	-24.62	-75.56	-8.00	-33.60	.4	3.25	442.0
4250	-23.98	-80.18	-7.00	-32.63	.8	3.25	442.0
4300	-23.43	-86.47	-6.00	-31.63	.8	3.25	442.0
4350	-23.32	-83.38	-5.00	-30.63	.8	3.25	442.0
4400	-23.54	-87.24	-4.00	-29.63	.8	3.25	442.0
4450	-23.96	-86.05	-3.00	-28.63	.9	3.25	442.0
4500	-24.21	-87.22	-2.00	-27.63	.9	3.25	442.0
4550	-24.37	-88.69	-1.00	-26.62	1.3	3.25	442.0
4600	-24.44	-90.88	0.00	-25.63	1.3	3.25	442.0
4650	-24.49	-84.00	1.00	-24.63	1.3	3.25	442.0
4700	-25.50	-80.61	2.00	-23.65	.8	3.25	442.0
4750	-25.53	-77.47	3.00	-22.64	1.2	3.25	442.0
4800	-24.12	-75.13	4.00	-21.65	1.2	3.25	442.0
4850	-23.42	-74.98	5.00	-20.68	1.1	3.25	442.0
4900	-22.49	-74.14	6.00	-19.72	1.2	3.25	441.5
4950	-21.92	-74.58	7.00	-18.75	1.2	3.25	441.0
5000	-21.46	-75.00	8.00	-17.85	1.3	3.25	441.0
5050	-21.56	-78.89	9.00	-17.01	2.3	3.25	441.0
5100	-22.17	-83.15	10.00	-16.08	2.3	3.25	441.0
5150	-21.51	-80.55	11.00	-15.16	2.4	3.24	440.5
5200	-21.25	-81.22	12.00	-14.27	2.1	3.24	440.0
5250	-21.84	-79.98	13.00	-13.27	2.5	3.24	440.0
5300	-21.98	-79.23	14.00	-12.40	2.6	3.24	439.5
5350	-22.68	-75.75	15.00	-11.57	2.7	3.24	439.0
5400	-22.45	-74.20	16.00	-10.77	2.9	3.23	438.0
5450	-22.41	-72.99	17.00	-9.99	3.1	3.23	438.0
5500	-22.59	-73.49	18.00	-9.26	3.3	3.23	437.0
5550	-23.11	-73.77	0.00	0.00	0.0	0.00	0.0
5600	-23.78	-75.57	0.00	0.00	0.0	0.00	0.0
5650	-23.76	-77.77	0.00	0.00	0.0	0.00	0.0
5700	-22.85	-76.59	0.00	0.00	0.0	0.00	0.0
5750	-23.10	-77.43	0.00	0.00	0.0	0.00	0.0
5800	-24.28	-77.65	0.00	0.00	0.0	0.00	0.0
5850	-24.23	-75.27	0.00	0.00	0.0	0.00	0.0
5900	-23.78	-75.51	0.00	0.00	0.0	0.00	0.0
5950	-22.33	-74.41	0.00	0.00	0.0	0.00	0.0
6000	-21.32	-74.80	0.00	0.00	0.0	0.00	0.0

SWITCH MATRIX
TRAY TEST

CROSSPOINT: #23

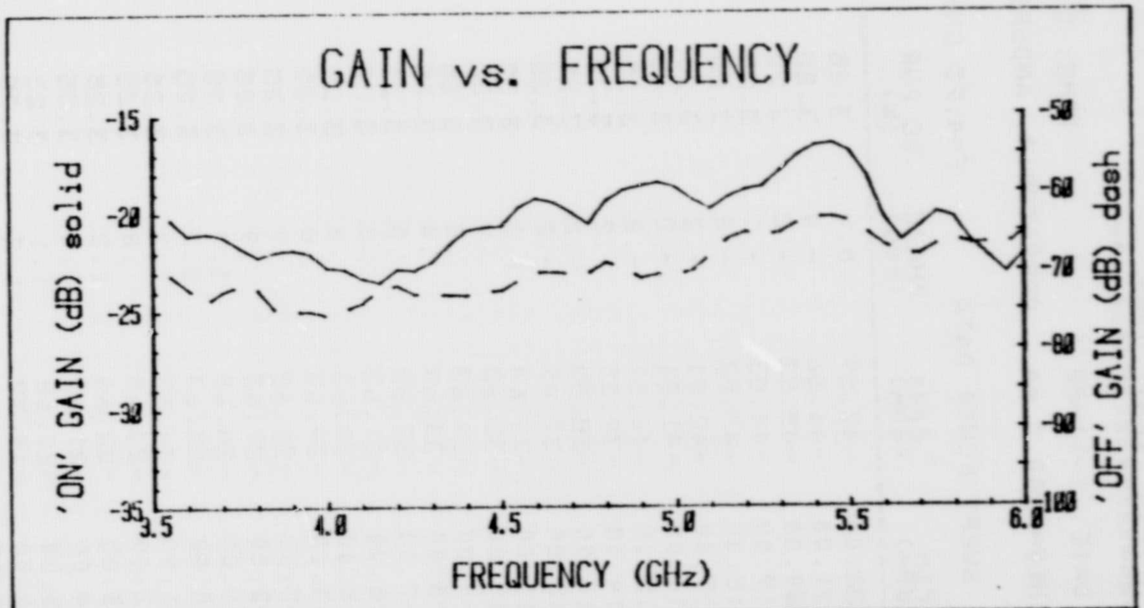
DATE: 11-4-82

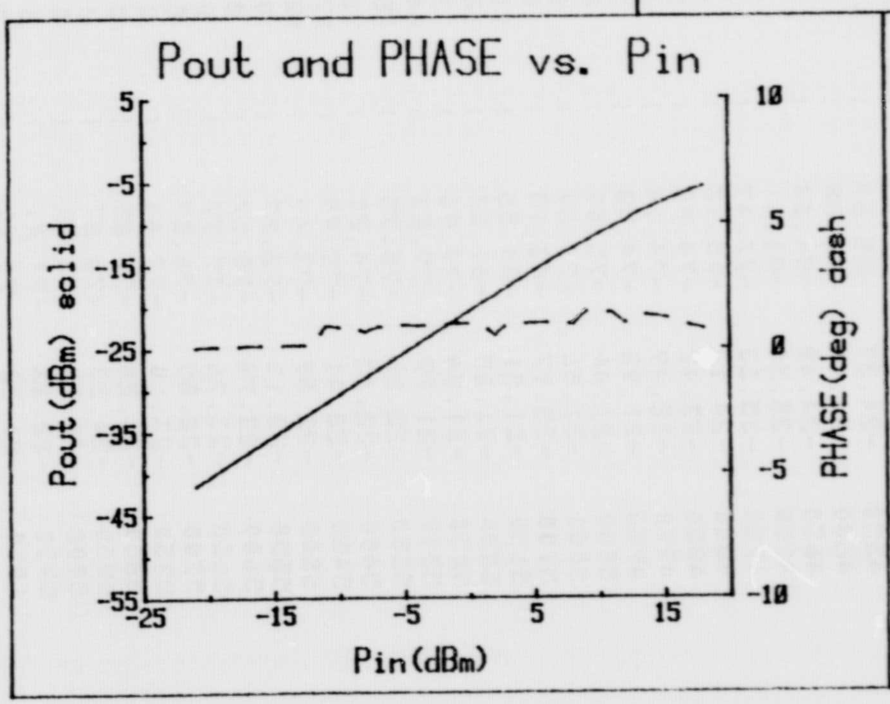
TIME: 10:30 AM

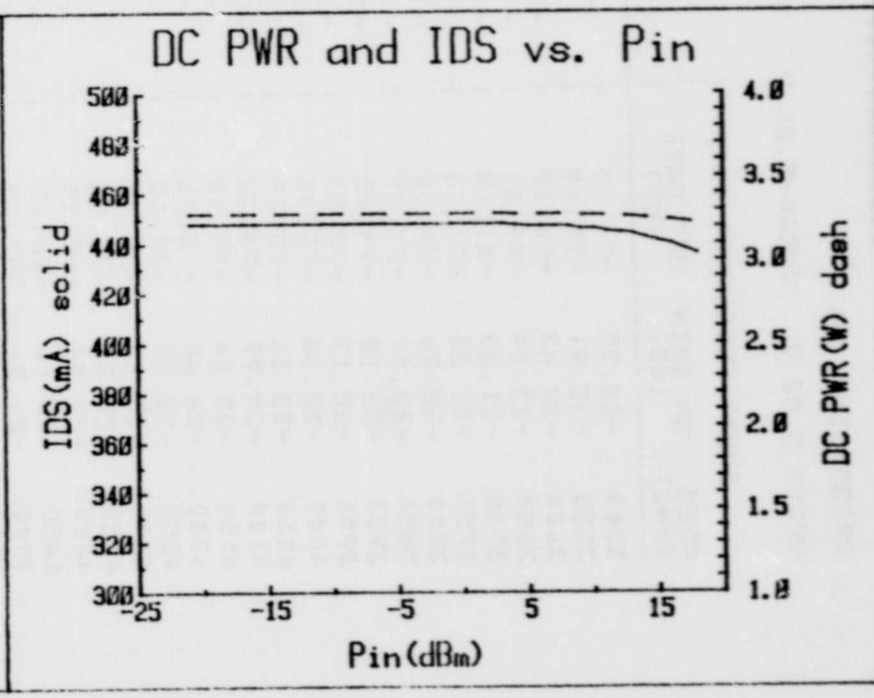
VPOS=5.0 V VNEG=-5.180 V

F=4.75GHZ INEG= 200.0 mA

OPERATOR: A. ANDERSON







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SWITCH MATRIX TRAY TEST

CROSSPOINT: #23 DATE: 11-4-82 TIME: 10:30 AM

VPOS= 5.01 V VNEG=-5.18 V INEG= 200.0 mA OPERATOR: A. ANDERSON

SWEPT FREQUENCY DATA			SWEPT POWER DATA			F=4.75 GHz.	
FREQ (MHz)	ON GAIN (dB)	OFF GAIN (dB)	Pin (dBm)	Pout (dBm)	PHASE (deg)	DC PWR (W)	IDS (mA)
3500	-19.90	-69.37	-22.00	-42.49	0.0	3.28	448.0
3550	-20.31	-70.33	-21.00	-41.47	.1	3.28	448.0
3600	-21.11	-72.01	-20.00	-40.46	.1	3.28	448.0
3650	-21.01	-73.86	-19.00	-39.46	.1	3.28	448.0
3700	-21.17	-72.37	-18.00	-38.47	.1	3.28	448.0
3750	-21.71	-71.62	-17.00	-37.47	.1	3.28	448.0
3800	-22.21	-72.13	-16.00	-36.47	.1	3.28	448.0
3850	-21.96	-74.74	-15.00	-35.46	.1	3.28	448.0
3900	-21.86	-75.01	-14.00	-34.47	.2	3.28	448.0
3950	-22.05	-75.02	-13.00	-33.46	.2	3.28	448.0
4000	-22.75	-75.56	-12.00	-32.47	.2	3.28	448.0
4050	-22.85	-74.79	-11.00	-31.53	.9	3.28	448.0
4100	-23.30	-73.99	-10.00	-30.52	.9	3.28	448.0
4150	-23.52	-72.08	-9.00	-29.53	.9	3.28	448.0
4200	-22.85	-71.67	-8.00	-28.53	.7	3.28	448.0
4250	-22.92	-72.83	-7.00	-27.53	.9	3.28	448.0
4300	-22.47	-72.90	-6.00	-26.53	.9	3.28	448.0
4350	-21.62	-72.98	-5.00	-25.54	.9	3.28	448.0
4400	-20.92	-73.03	-4.00	-24.54	.9	3.28	448.0
4450	-20.74	-72.51	-3.00	-23.55	.9	3.28	448.0
4500	-20.68	-72.45	-2.00	-22.57	1.0	3.28	448.0
4550	-19.72	-71.08	-1.00	-21.57	1.0	3.28	448.0
4600	-19.30	-70.12	0.00	-20.58	1.0	3.28	448.0
4650	-19.49	-70.09	1.00	-19.60	1.0	3.28	448.0
4700	-19.99	-70.30	2.00	-18.66	.5	3.28	448.0
4750	-20.58	-70.23	3.00	-17.63	1.0	3.28	448.0
4800	-19.43	-68.86	4.00	-16.66	1.0	3.28	447.5
4850	-18.87	-69.52	5.00	-15.70	1.0	3.28	447.0
4900	-18.65	-70.83	6.00	-14.74	1.0	3.28	447.0
4950	-18.48	-70.39	7.00	-13.80	1.0	3.28	447.0
5000	-18.74	-70.53	8.00	-13.00	1.0	3.28	447.0
5050	-19.36	-69.86	9.00	-12.14	1.5	3.27	446.0
5100	-19.83	-67.95	10.00	-11.29	1.4	3.27	446.0
5150	-19.25	-65.90	11.00	-10.49	1.4	3.27	445.0
5200	-18.87	-65.12	12.00	-9.76	1.0	3.26	444.5
5250	-18.70	-65.52	13.00	-8.75	1.3	3.26	444.0
5300	-17.91	-65.16	14.00	-8.09	1.3	3.25	442.5
5350	-17.11	-63.93	15.00	-7.46	1.2	3.25	441.0
5400	-16.62	-63.25	16.00	-6.84	1.1	3.24	440.0
5450	-16.49	-63.20	17.00	-6.24	.9	3.23	438.0
5500	-16.92	-63.67	18.00	-5.68	.8	3.22	436.0
5550	-18.17	-65.12	0.00	0.00	0.0	0.00	0.0
5600	-20.30	-66.72	0.00	0.00	0.0	0.00	0.0
5650	-21.44	-67.88	0.00	0.00	0.0	0.00	0.0
5700	-20.78	-67.94	0.00	0.00	0.0	0.00	0.0
5750	-20.04	-66.67	0.00	0.00	0.0	0.00	0.0
5800	-20.31	-65.99	0.00	0.00	0.0	0.00	0.0
5850	-21.52	-66.62	0.00	0.00	0.0	0.00	0.0
5900	-22.31	-66.46	0.00	0.00	0.0	0.00	0.0
5950	-23.10	-66.68	0.00	0.00	0.0	0.00	0.0
6000	-22.17	-65.32	0.00	0.00	0.0	0.00	0.0

HEWLETT PACKARD

SWITCH MATRIX
TRAY TEST

CROSSPOINT: #31

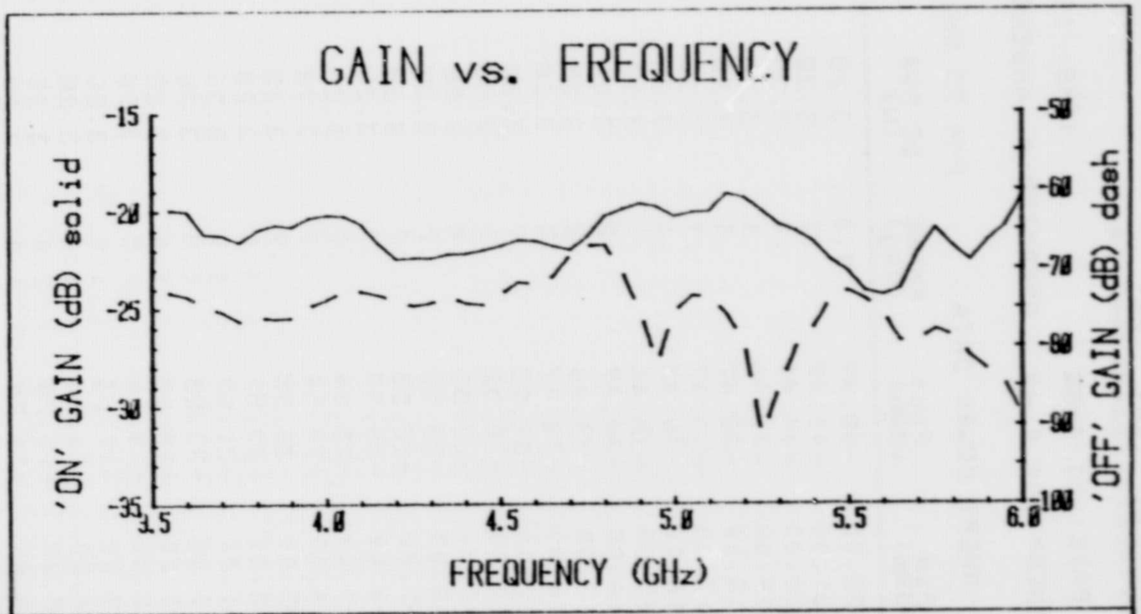
DATE: 1-11-82

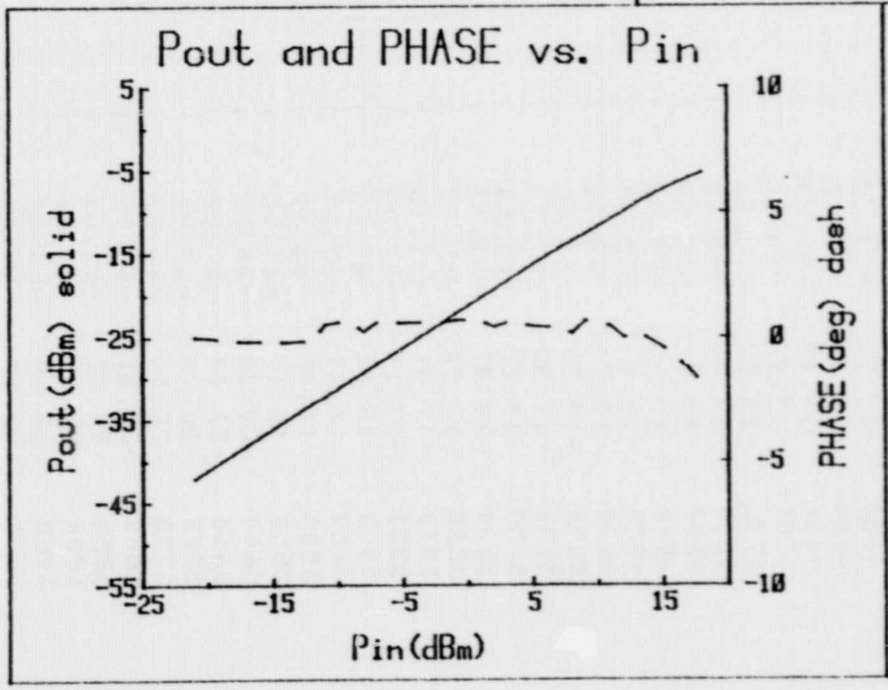
TIME: 2:52 PM

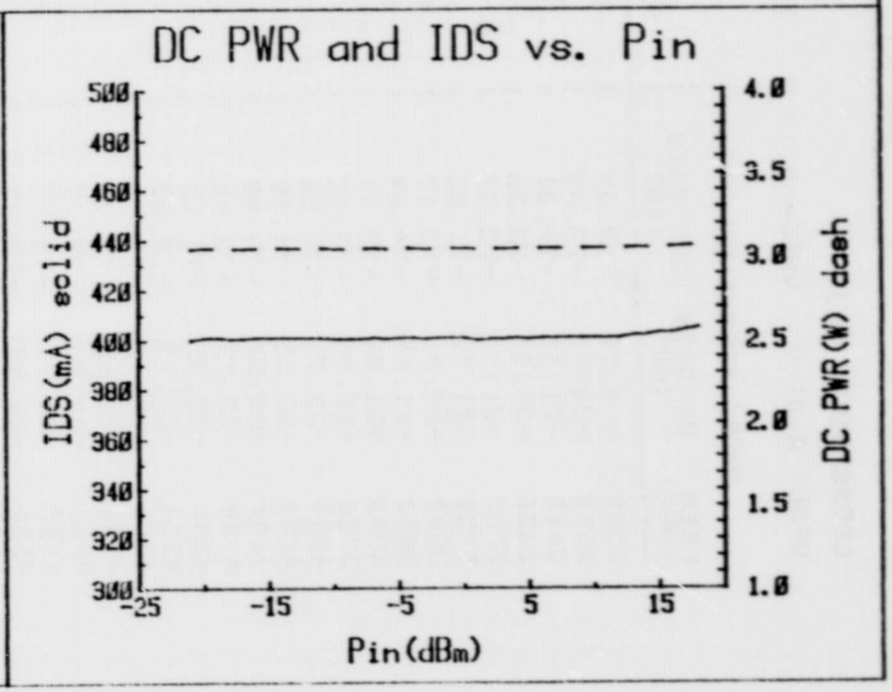
VPOS=5.0 V VNEG=-5.210 V

F=4.75GHZ INEG= 200.0 mA

OPERATOR: A. ANDERSON







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SWITCH MATRIX TRAY TEST

CROSSPOINT: #31 DATE: 1-11-82 TIME: 2:52 PM

VPOS= 5.01 V VNEG=-5.21 V INEG= 200.0 mA OPERATOR:A. ANDERSON

SWEPT FREQUENCY DATA			SWEPT POWER DATA			F=4.75 GHz.	
FREQ (MHz)	ON GAIN (dB)	OFF GAIN (dB)	Pin (dBm)	Pout (dBm)	PHASE (deg)	DC PWR (W)	IDS (mA)
3500	-20.64	-76.31	-22.00	-43.11	0.0	3.05	401.0
3550	-19.94	-72.92	-21.00	-42.08	-.0	3.05	400.0
3600	-20.02	-73.43	-20.00	-41.08	-.0	3.05	401.0
3650	-21.16	-74.70	-19.00	-40.07	-.1	3.05	401.0
3700	-21.23	-75.43	-18.00	-39.07	-.2	3.05	400.5
3750	-21.58	-76.63	-17.00	-38.07	-.2	3.05	400.5
3800	-20.97	-76.11	-16.00	-37.08	-.2	3.05	401.0
3850	-20.69	-76.31	-15.00	-36.09	-.2	3.05	401.0
3900	-20.80	-76.16	-14.00	-35.09	-.2	3.05	401.0
3950	-20.34	-74.70	-13.00	-34.09	-.2	3.05	401.0
4000	-20.22	-73.89	-12.00	-33.08	-.2	3.05	401.0
4050	-20.25	-72.74	-11.00	-32.29	.5	3.05	401.0
4100	-20.67	-72.82	-10.00	-31.30	.6	3.05	400.5
4150	-21.64	-73.26	-9.00	-30.29	.6	3.05	400.5
4200	-22.45	-74.10	-8.00	-29.31	.2	3.05	400.5
4250	-22.39	-74.65	-7.00	-28.30	.6	3.05	401.0
4300	-22.41	-74.29	-6.00	-27.30	.6	3.05	400.5
4350	-22.20	-73.51	-5.00	-26.30	.6	3.05	401.0
4400	-22.18	-74.36	-4.00	-25.30	.6	3.05	401.0
4450	-22.01	-74.55	-3.00	-24.31	.6	3.05	400.5
4500	-21.80	-73.27	-2.00	-23.31	.6	3.05	401.0
4550	-21.50	-71.68	-1.00	-22.23	.7	3.05	401.0
4600	-21.55	-71.89	0.00	-21.24	.7	3.05	401.0
4650	-21.80	-70.99	1.00	-20.25	.6	3.05	400.0
4700	-22.01	-68.23	2.00	-19.27	.4	3.05	400.5
4750	-21.32	-67.01	3.00	-18.26	.6	3.05	400.5
4800	-20.29	-66.88	4.00	-17.27	.5	3.05	401.0
4850	-19.95	-70.42	5.00	-16.31	.4	3.05	400.5
4900	-19.68	-75.24	6.00	-15.33	.4	3.05	401.0
4950	-19.85	-82.06	7.00	-14.37	.4	3.05	401.0
5000	-20.32	-75.45	8.00	-13.49	.1	3.05	401.0
5050	-20.12	-73.48	9.00	-12.67	.6	3.05	401.0
5100	-20.06	-73.57	10.00	-11.76	.5	3.05	401.0
5150	-19.18	-75.86	11.00	-10.85	.4	3.05	401.0
5200	-19.37	-79.42	12.00	-10.00	-.0	3.05	401.0
5250	-20.02	-91.16	13.00	-8.98	.2	3.06	402.0
5300	-20.72	-85.16	14.00	-8.16	-.1	3.06	402.0
5350	-21.08	-80.00	15.00	-7.38	-.4	3.06	403.0
5400	-21.59	-77.44	16.00	-6.64	-.9	3.06	403.0
5450	-22.52	-73.82	17.00	-5.96	-1.3	3.07	404.0
5500	-23.13	-72.84	18.00	-5.36	-1.9	3.07	405.0
5550	-24.14	-73.91	0.00	0.00	0.0	0.00	0.0
5600	-24.35	-75.76	0.00	0.00	0.0	0.00	0.0
5650	-24.02	-79.20	0.00	0.00	0.0	0.00	0.0
5700	-22.16	-79.21	0.00	0.00	0.0	0.00	0.0
5750	-20.91	-77.81	0.00	0.00	0.0	0.00	0.0
5800	-21.83	-78.62	0.00	0.00	0.0	0.00	0.0
5850	-22.56	-81.15	0.00	0.00	0.0	0.00	0.0
5900	-21.57	-82.91	0.00	0.00	0.0	0.00	0.0
5950	-20.82	-84.56	0.00	0.00	0.0	0.00	0.0
6000	-19.35	-88.66	0.00	0.00	0.0	0.00	0.0

HEWLETT PACKARD

SWITCH MATRIX TRAY TEST

CROSSPOINT: #45

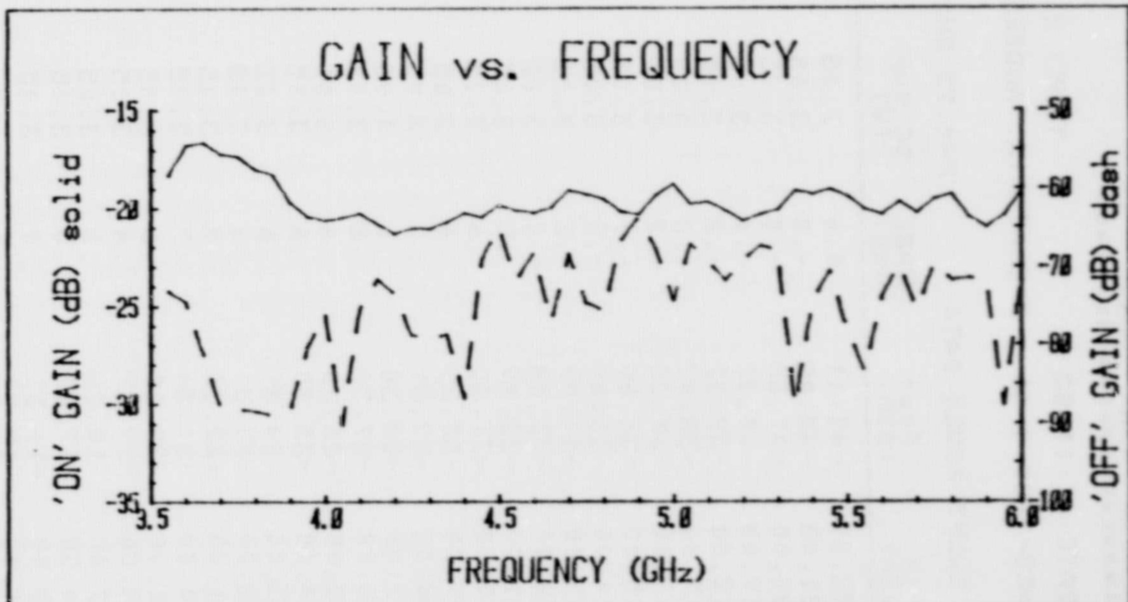
DATE: 11-4-82

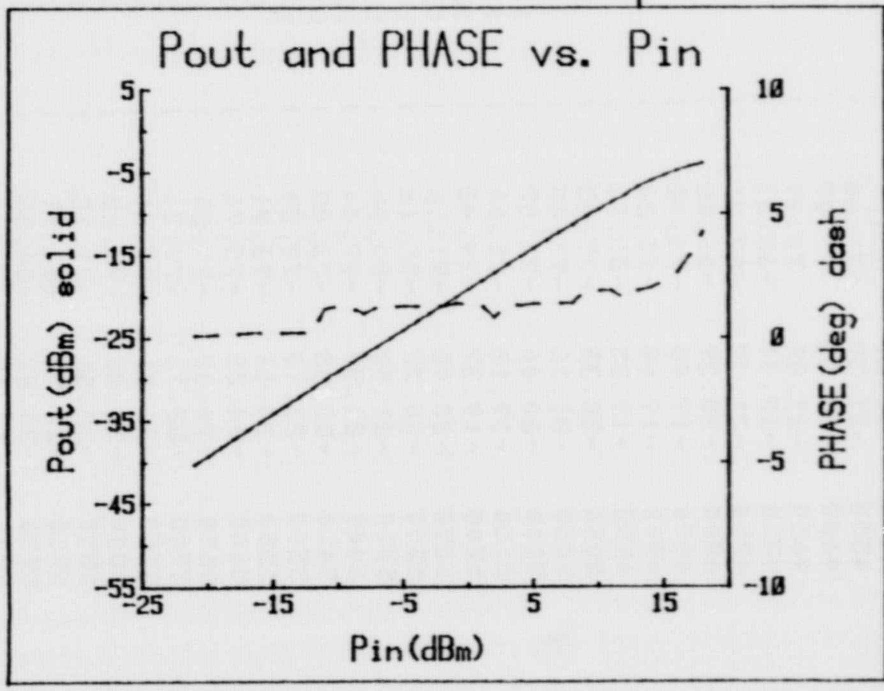
TIME: 10:48 AM

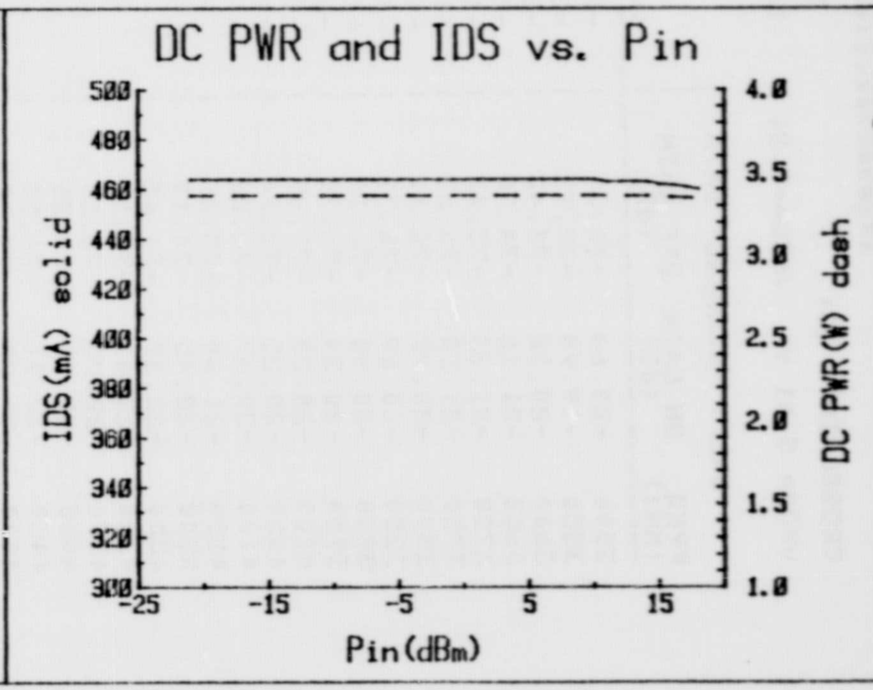
VPOS=5.Ø V VNEG=-5.19Ø V

F=4.75GHZ INEG= 2ØØ.Ø mA

OPERATOR: A. ANDERSON







SWITCH MATRIX TRAY TEST

CROSSPOINT: #45 DATE: 11-4-82 TIME: 10:48 AM

VPOS= 5.01 V VNEG=-5.19 V INEG= 200.0 mA OPERATOR:A. ANDERSON

SWEPT FREQUENCY DATA			SWEPT POWER DATA		F=4.75 GHz.		
FREQ (MHz)	ON GAIN (dB)	OFF GAIN (dB)	Pin (dBm)	Pout (dBm)	PHASE (deg)	DC PWR (W)	IDS (mA)
3500	-18.62	-74.81	-22.00	-41.33	0.0	3.36	464.0
3550	-18.27	-73.05	-21.00	-40.29	.1	3.36	464.0
3600	-16.76	-74.39	-20.00	-39.27	.1	3.36	464.0
3650	-16.61	-81.01	-19.00	-38.27	.1	3.36	464.0
3700	-17.21	-87.84	-18.00	-37.27	.2	3.36	464.0
3750	-17.33	-88.13	-17.00	-36.27	.2	3.36	464.0
3800	-18.00	-88.45	-16.00	-35.26	.2	3.36	464.0
3850	-18.26	-88.94	-15.00	-34.26	.2	3.36	464.0
3900	-19.70	-88.13	-14.00	-33.26	.2	3.36	464.0
3950	-20.44	-80.14	-13.00	-32.25	.2	3.36	464.0
4000	-20.64	-75.84	-12.00	-31.24	.3	3.36	464.0
4050	-20.49	-90.10	-11.00	-30.14	1.2	3.36	464.0
4100	-20.27	-75.26	-10.00	-29.13	1.3	3.36	464.0
4150	-20.80	-71.53	-9.00	-28.13	1.2	3.36	464.0
4200	-21.33	-73.38	-8.00	-27.13	1.0	3.36	464.0
4250	-21.05	-78.69	-7.00	-26.14	1.2	3.36	464.0
4300	-21.08	-79.14	-6.00	-25.13	1.2	3.36	464.0
4350	-20.73	-78.61	-5.00	-24.13	1.3	3.36	464.0
4400	-20.28	-86.74	-4.00	-23.13	1.3	3.36	464.0
4450	-20.48	-69.10	-3.00	-22.13	1.3	3.36	464.0
4500	-19.87	-64.98	-2.00	-21.13	1.3	3.36	464.0
4550	-20.13	-71.65	-1.00	-20.18	1.4	3.36	464.0
4600	-20.26	-68.24	0.00	-19.18	1.4	3.36	464.0
4650	-19.97	-76.87	1.00	-18.20	1.3	3.36	464.0
4700	-19.10	-68.39	2.00	-17.24	.8	3.36	464.0
4750	-19.31	-74.55	3.00	-16.21	1.3	3.36	464.0
4800	-19.54	-75.54	4.00	-15.22	1.3	3.36	464.0
4850	-20.20	-66.68	5.00	-14.24	1.4	3.36	464.0
4900	-20.36	-63.80	6.00	-13.26	1.4	3.36	464.0
4950	-19.34	-67.70	7.00	-12.30	1.4	3.36	464.0
5000	-18.77	-74.19	8.00	-11.42	1.4	3.36	464.0
5050	-19.81	-67.16	9.00	-10.42	1.9	3.36	464.0
5100	-19.69	-69.33	10.00	-9.51	1.9	3.36	464.0
5150	-20.14	-71.72	11.00	-8.64	1.9	3.36	463.0
5200	-20.69	-69.25	12.00	-7.81	1.6	3.36	463.0
5250	-20.35	-67.40	13.00	-6.78	1.9	3.36	463.0
5300	-20.12	-67.94	14.00	-6.06	2.0	3.36	463.0
5350	-19.12	-87.80	15.00	-5.41	2.2	3.35	462.0
5400	-19.30	-74.28	16.00	-4.86	2.6	3.35	461.5
5450	-19.04	-70.55	17.00	-4.37	3.3	3.35	461.0
5500	-19.39	-78.02	18.00	-3.95	4.3	3.34	460.0
5550	-20.08	-83.44	0.00	0.00	0.0	0.00	0.0
5600	-20.36	-73.58	0.00	0.00	0.0	0.00	0.0
5650	-19.69	-69.80	0.00	0.00	0.0	0.00	0.0
5700	-20.28	-75.41	0.00	0.00	0.0	0.00	0.0
5750	-19.54	-69.55	0.00	0.00	0.0	0.00	0.0
5800	-19.29	-71.70	0.00	0.00	0.0	0.00	0.0
5850	-20.49	-71.42	0.00	0.00	0.0	0.00	0.0
5900	-21.01	-71.95	0.00	0.00	0.0	0.00	0.0
5950	-20.42	-87.63	0.00	0.00	0.0	0.00	0.0
6000	-19.19	-71.64	0.00	0.00	0.0	0.00	0.0

SWITCH MATRIX
TRAY TEST

CROSSPOINT: #66

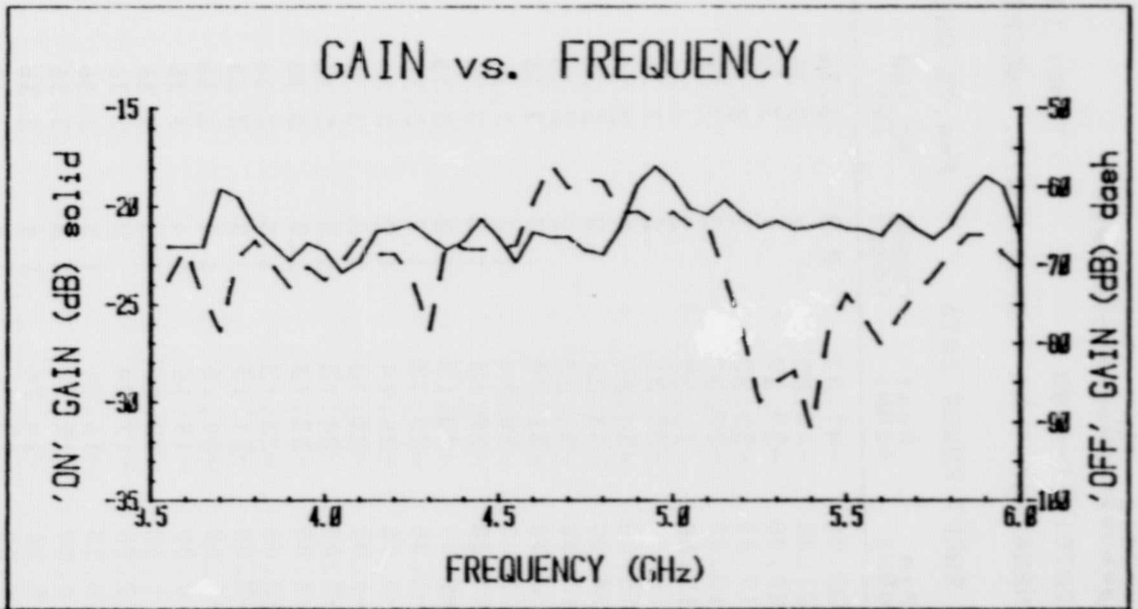
DATE: 11-1-82

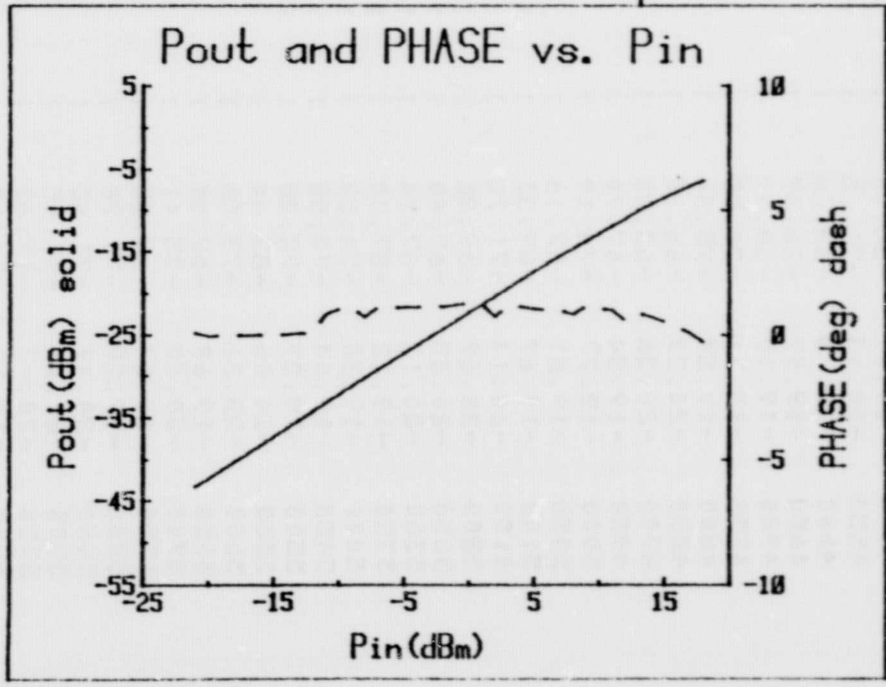
TIME: 5:00 PM

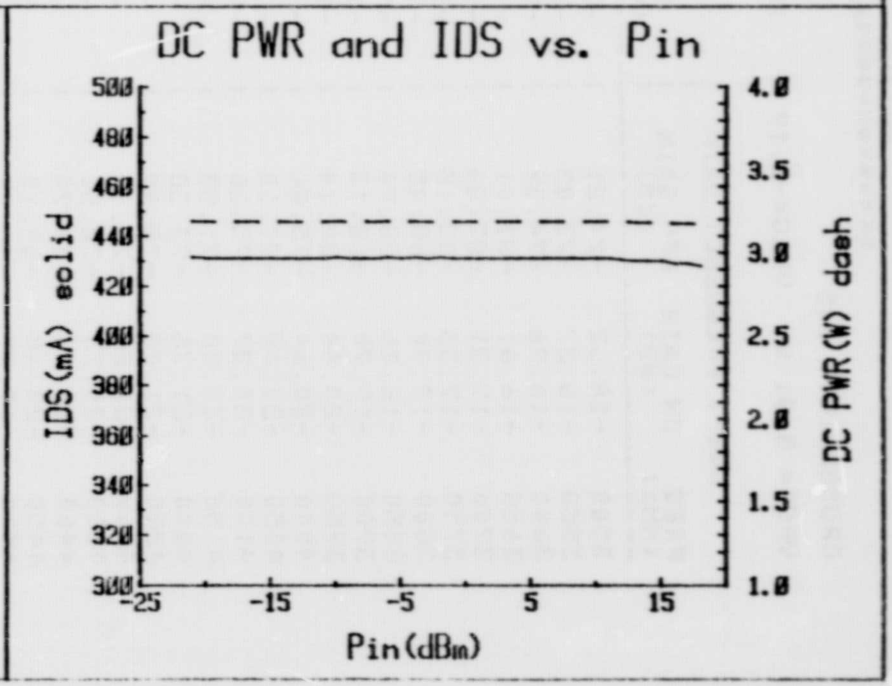
VPOS=5.0 V VNEG=-5.170 V

F=4.75GHZ INEG= 200.0 mA

OPERATOR: J. PELOSE







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SWITCH MATRIX TRAY TEST

CROSSPOINT: #66 DATE: 11-1-82 TIME: 5:00 PM

VPOS= 4.99 V VNEG=-5.17 V INEG= 200.0 mA OPERATOR: J. PELOSE

SWEPT FREQUENCY DATA			SWEPT POWER DATA		F=4.75 GHz.		
FREQ (MHz)	ON GAIN (dB)	OFF GAIN (dB)	Pin (dBm)	Pout (dBm)	PHASE (deg)	DC PWR (W)	IDS (mA)
3500	-22.55	-83.02	-22.00	-44.35	0.0	3.18	431.0
3550	-22.09	-71.90	-21.00	-43.33	.1	3.19	431.5
3600	-22.10	-67.91	-20.00	-42.30	-.1	3.18	431.0
3650	-22.10	-73.98	-19.00	-41.30	-.0	3.18	431.0
3700	-19.10	-78.39	-18.00	-40.30	-.0	3.18	431.0
3750	-19.55	-69.14	-17.00	-39.29	-.0	3.18	431.0
3800	-21.15	-66.90	-16.00	-38.30	-.0	3.18	431.0
3850	-21.96	-70.11	-15.00	-37.29	-.0	3.18	431.0
3900	-22.78	-72.81	-14.00	-36.29	.0	3.18	431.0
3950	-21.92	-70.25	-13.00	-35.29	.1	3.18	431.0
4000	-22.26	-71.89	-12.00	-34.29	.1	3.18	431.0
4050	-23.37	-69.56	-11.00	-33.27	.8	3.18	431.0
4100	-22.83	-66.73	-10.00	-32.28	1.0	3.19	431.5
4150	-21.27	-68.67	-9.00	-31.27	1.1	3.18	431.0
4200	-21.17	-68.63	-8.00	-30.27	.7	3.18	431.0
4250	-20.90	-71.38	-7.00	-29.27	1.1	3.18	431.0
4300	-21.60	-78.41	-6.00	-28.29	1.1	3.19	431.5
4350	-22.22	-67.04	-5.00	-27.28	1.1	3.18	431.0
4400	-21.77	-68.01	-4.00	-26.28	1.1	3.19	431.5
4450	-20.64	-68.05	-3.00	-25.29	1.2	3.18	431.0
4500	-21.59	-67.88	-2.00	-24.29	1.1	3.19	431.5
4550	-22.85	-67.49	-1.00	-23.33	1.2	3.18	431.0
4600	-21.33	-61.79	0.00	-22.34	1.3	3.18	431.0
4650	-21.60	-56.95	1.00	-21.35	1.2	3.18	431.0
4700	-21.58	-60.07	2.00	-20.37	.7	3.18	431.0
4750	-22.27	-59.03	3.00	-19.36	1.2	3.18	431.0
4800	-22.47	-59.18	4.00	-18.38	1.1	3.18	431.0
4850	-21.08	-63.36	5.00	-17.41	1.0	3.18	431.0
4900	-18.81	-63.16	6.00	-16.46	1.0	3.18	431.0
4950	-17.90	-64.69	7.00	-15.50	1.0	3.18	431.0
5000	-18.73	-63.18	8.00	-14.64	.8	3.18	431.0
5050	-20.09	-64.90	9.00	-13.73	1.2	3.18	431.0
5100	-20.41	-64.70	10.00	-12.83	1.0	3.18	431.0
5150	-19.64	-71.31	11.00	-11.95	1.0	3.18	431.0
5200	-20.50	-78.28	12.00	-11.12	.6	3.18	430.5
5250	-21.09	-87.44	13.00	-10.09	.9	3.18	430.0
5300	-20.77	-84.78	14.00	-9.27	.7	3.18	430.0
5350	-21.18	-83.46	15.00	-8.49	.5	3.18	430.0
5400	-21.08	-90.92	16.00	-7.74	.3	3.17	429.0
5450	-20.86	-77.92	17.00	-7.02	.1	3.17	429.0
5500	-21.15	-73.65	18.00	-6.37	-.3	3.17	428.0
5550	-21.22	-76.69	0.00	0.00	0.0	0.00	0.0
5600	-21.51	-80.07	0.00	0.00	0.0	0.00	0.0
5650	-20.45	-76.49	0.00	0.00	0.0	0.00	0.0
5700	-21.17	-73.58	0.00	0.00	0.0	0.00	0.0
5750	-21.69	-71.26	0.00	0.00	0.0	0.00	0.0
5800	-20.93	-68.39	0.00	0.00	0.0	0.00	0.0
5850	-19.44	-66.15	0.00	0.00	0.0	0.00	0.0
5900	-18.43	-66.15	0.00	0.00	0.0	0.00	0.0
5950	-18.96	-68.59	0.00	0.00	0.0	0.00	0.0
6000	-21.47	-70.35	0.00	0.00	0.0	0.00	0.0

3.3.2

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF OF CONCEPT

TEST DATA SHEET #13

OUTPUT VSWR (RETURN LOSS) TEST

Test Conditions:	Frequency 3.0 GHz to 7.0 GHz	
	RF Signal Level:	Max -10 dBm (applied at the output ports)
	Input ports:	50 ohm terminated
	Switching mode:	One crosspoint per column turned "ON".
Test Procedure:	The return loss measurement shall be performed on the network analyzer in the sweep mode to cover the frequency band of 3 to 7 GHz. Attach plots or photographs for return loss vs frequency.	
Test Setup:	See Figure 3.3.2.1.	

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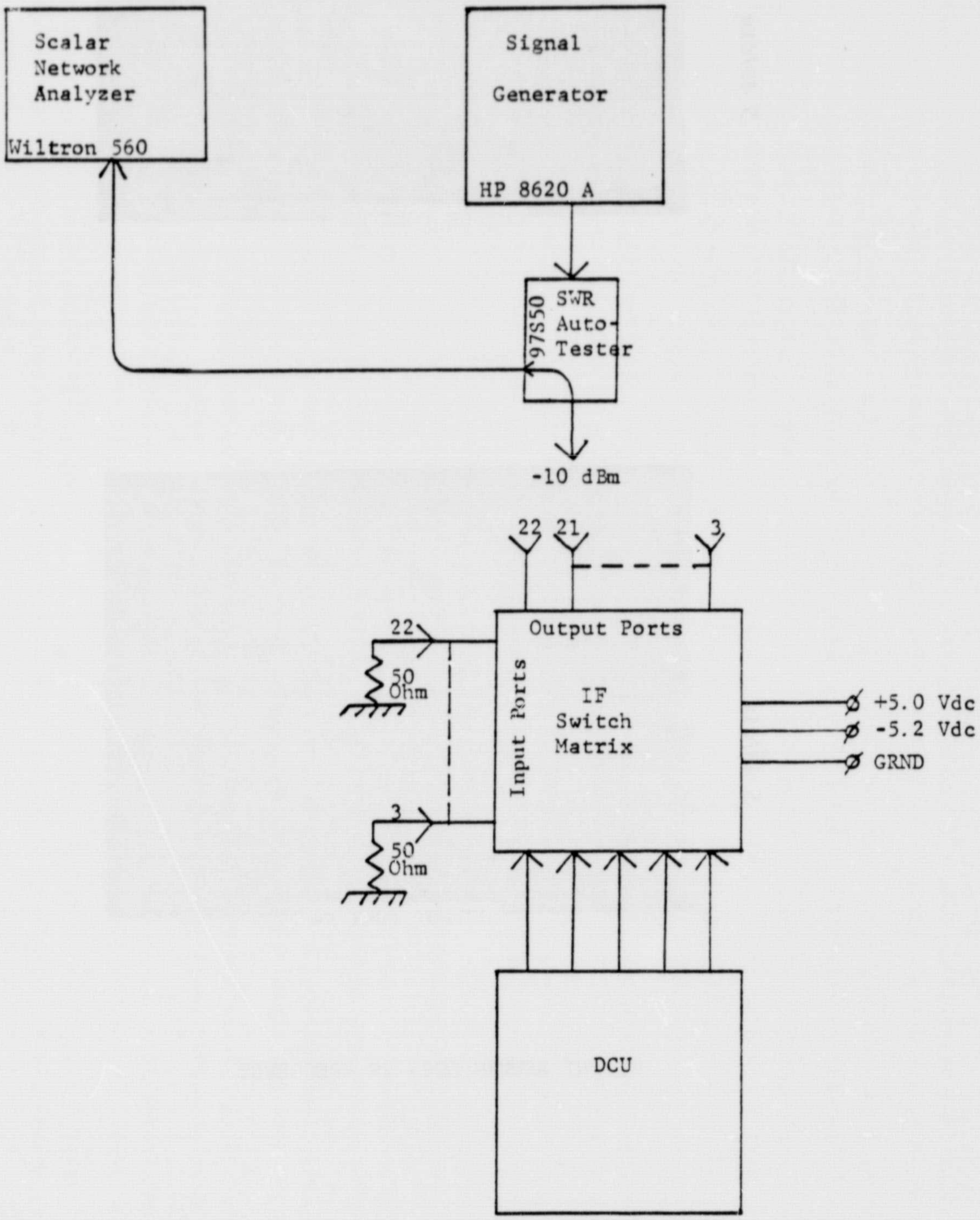
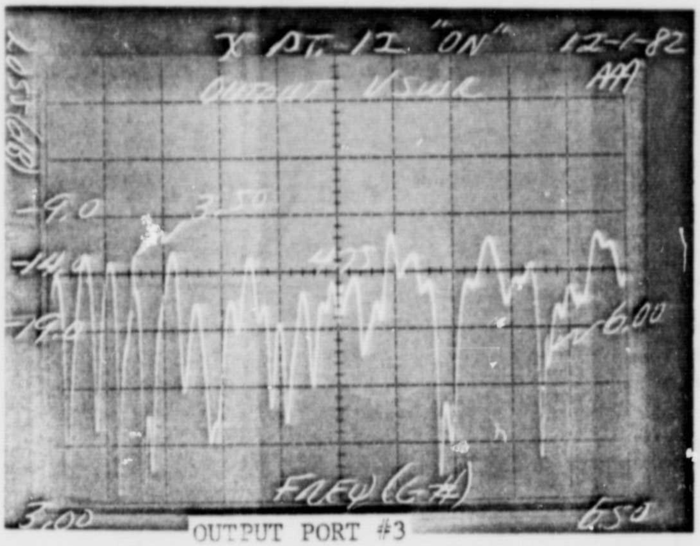
FIGURE 3.3.2.1



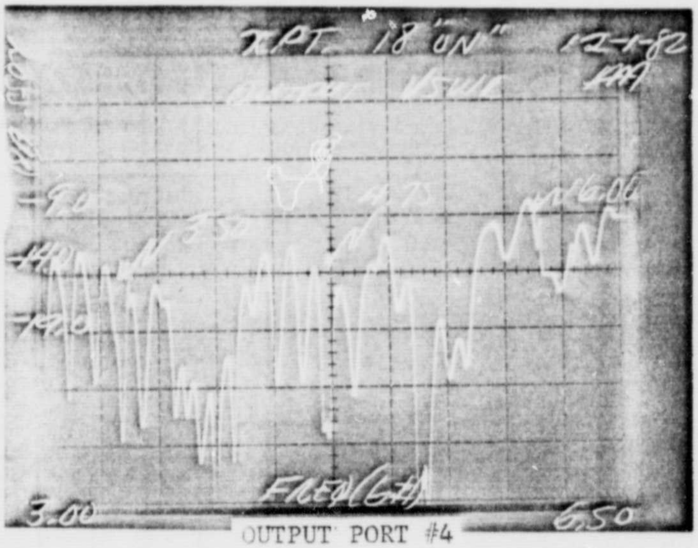
OUTPUT VSWR TEST SET-UP

5 dB/div



OUTPUT PORT #3

5 dB/div



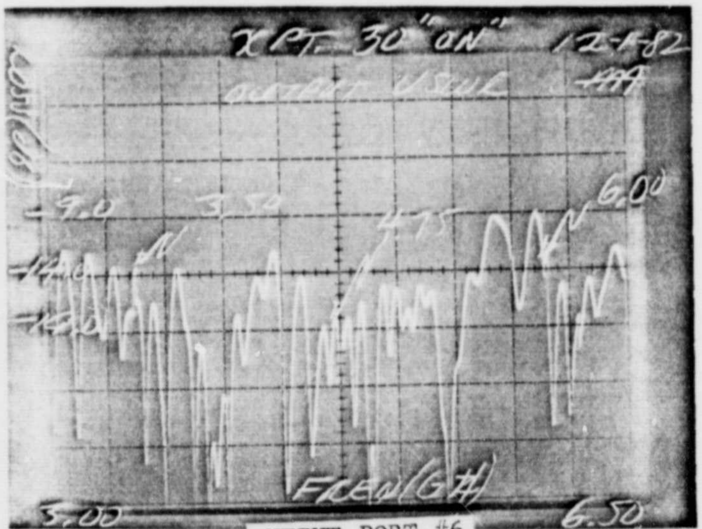
OUTPUT PORT #4

OUTPUT RETURN LOSS VS FREQUENCY

5 dB/div

OUTPUT PORT #5

5 dB/div



OUTPUT PORT #6

OUTPUT RETURN LOSS VS FREQUENCY

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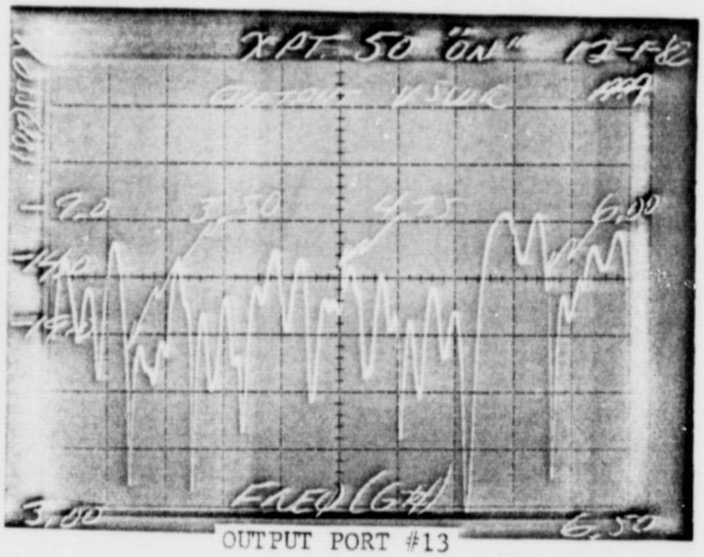
5 dB/div

OUTPUT PORT #7

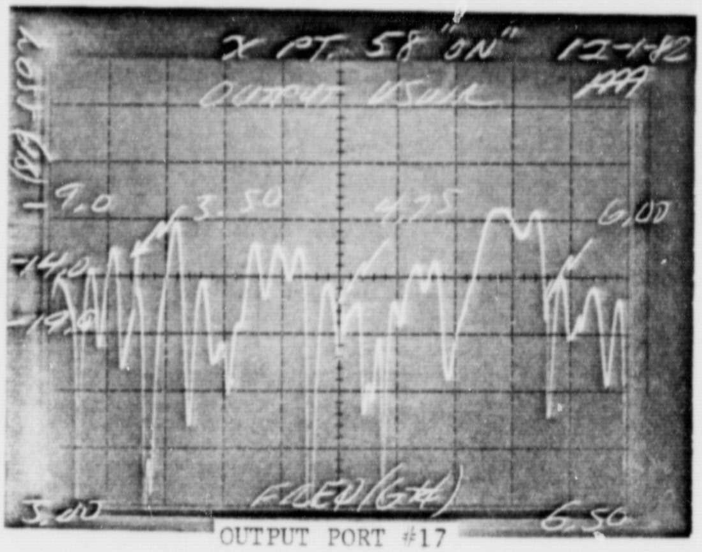
5 dB/div



OUTPUT PORT #13

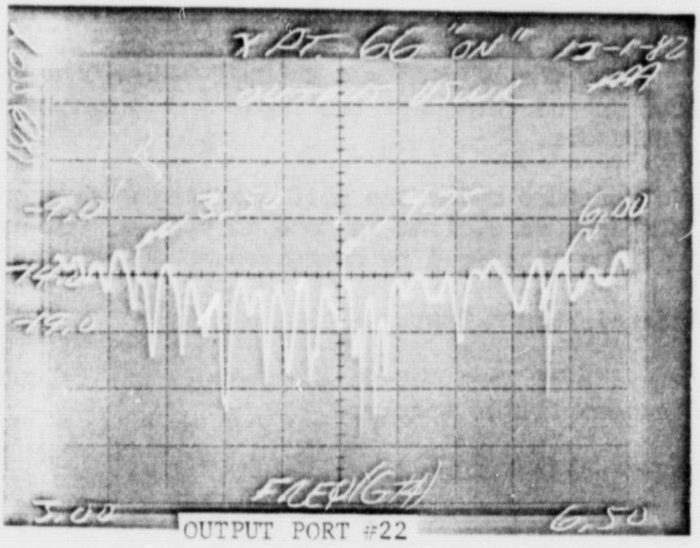
OUTPUT RETURN LOSS VS FREQUENCY

5 dB/div



OUTPUT PORT #17

5 dB/div



OUTPUT PORT #22

OUTPUT RETURN LOSS VS FREQUENCY

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3.3.3

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #12

THERMAL VACUUM TEST

TEST DESCRIPTION

1. Initial Functional Test

   Calibrate the RF Test Set-up and measure consumption and the frequency response of the switch amplifier module for an input RF level of -10 dBm maximum.

2. Thermal Vacuum Test

   2.1 Install the unit in the thermal vacuum chamber. Connect DC cables and terminate the input and output ports with 50 ohm resistors.

   2.2 Temperature cycle the unit starting with a cold start. The temperature cycling is done in vacuum. DC current consumptions will be monitored to detect anomalous operations.

3. Post Thermal-Vacuum Test

   Calibrate the RF Test Set-up and measure the frequency response of the switch-amplifier module.

4. Test Setup: See Figure 3.3.3.1.

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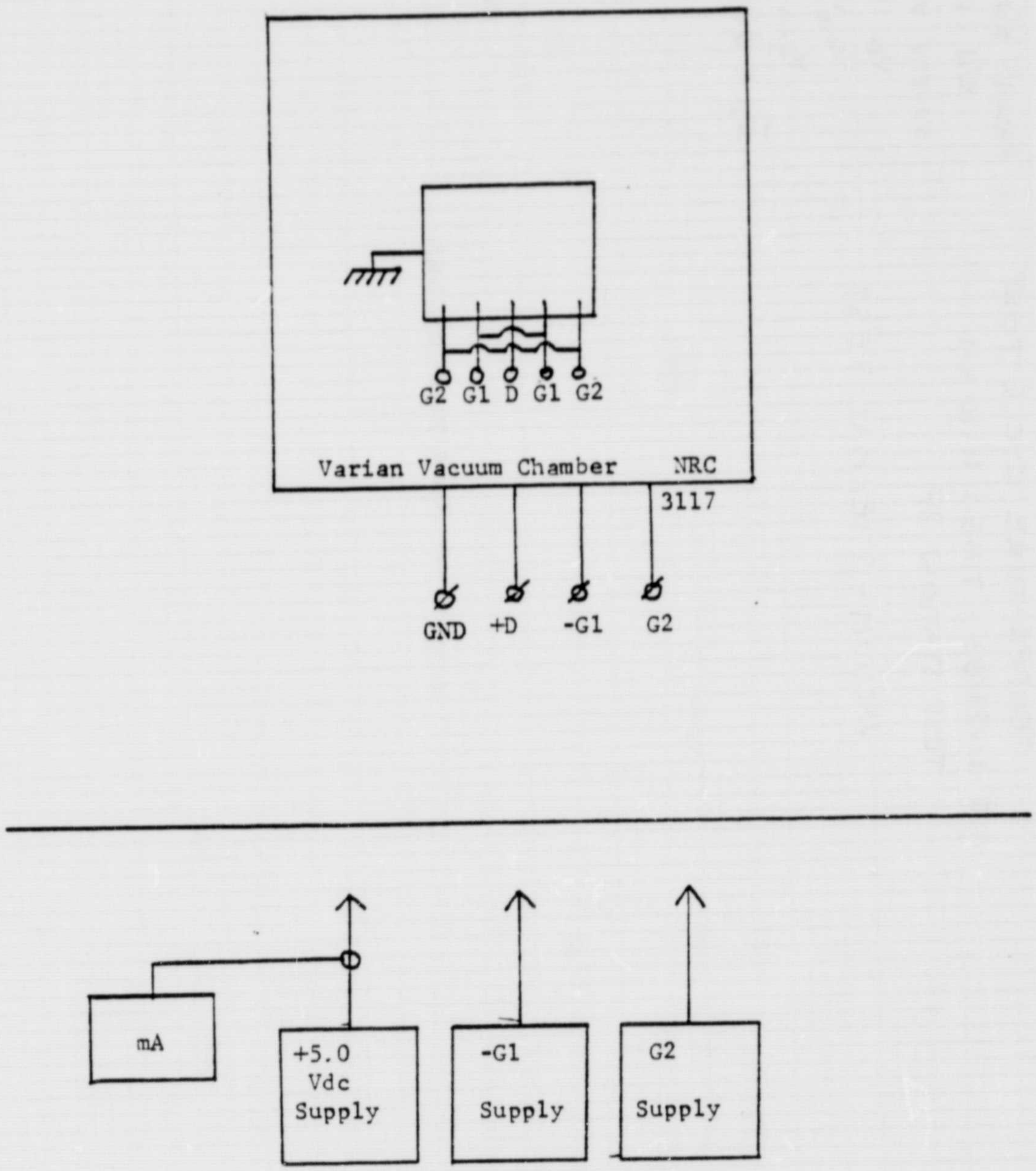
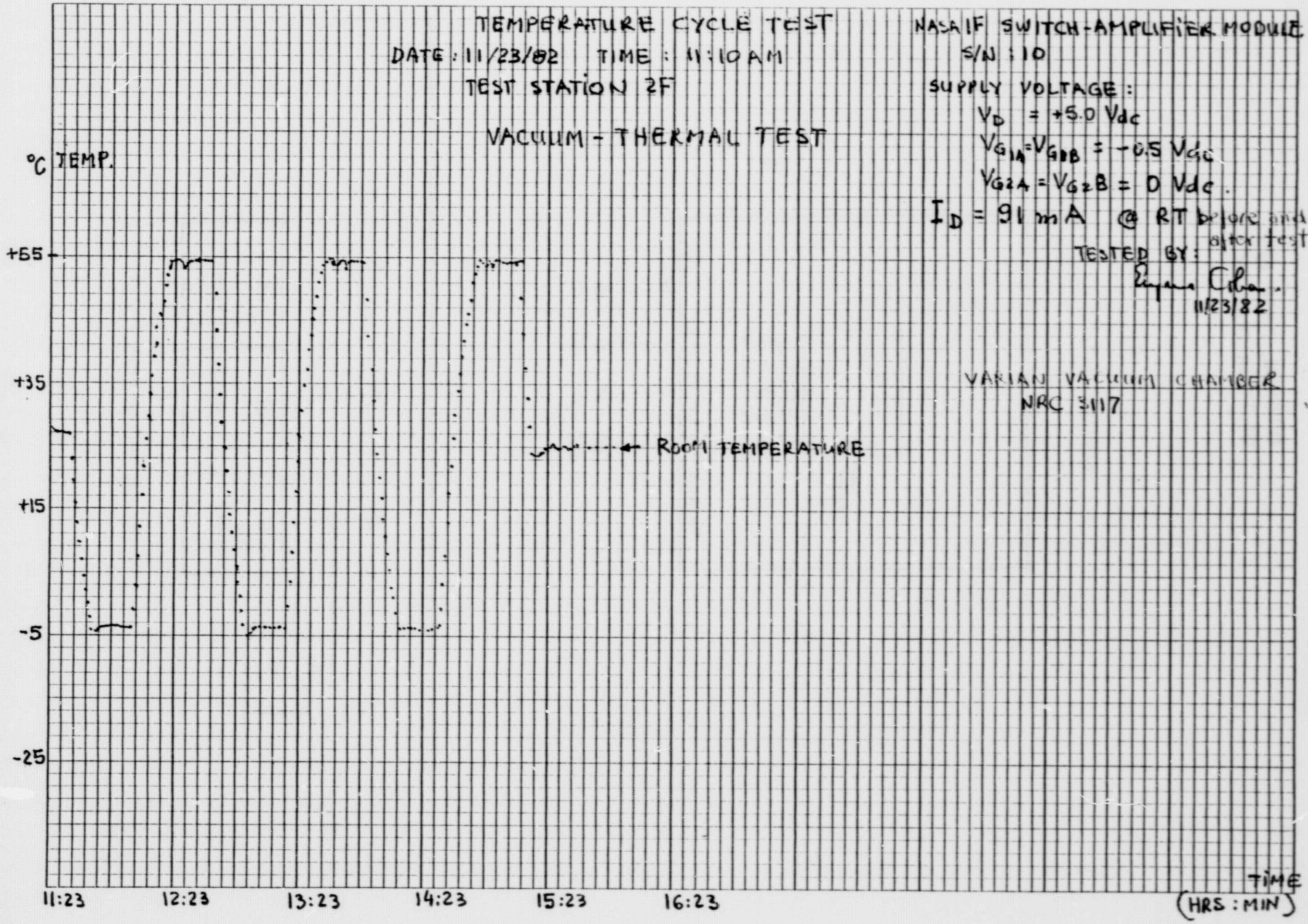
FIGURE 3.3.3.1



THERMAL VACUUM TEST

NO. 340R-10 DIETZGEN GRAPH PAPER
10 X 10 PER INCH

DIETZGEN CORPORATION
MADE IN U.S.A.



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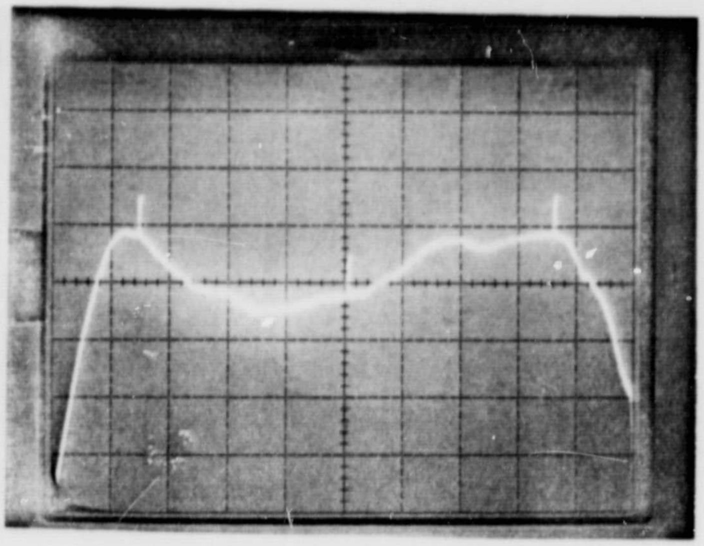
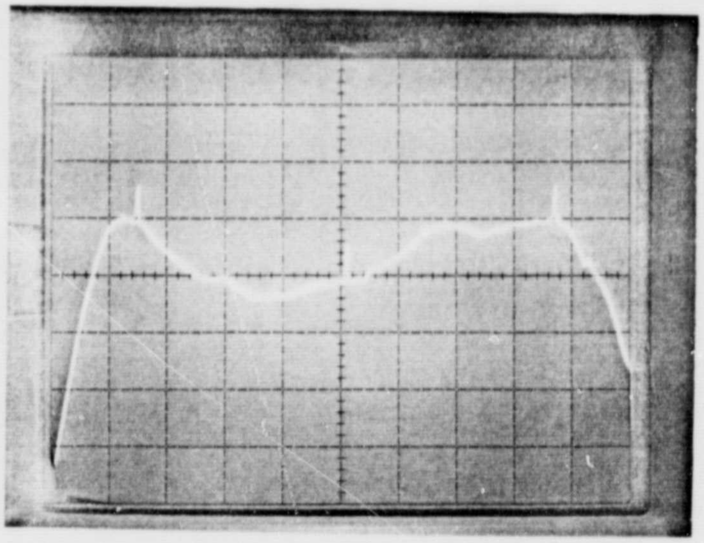
2 dB/div



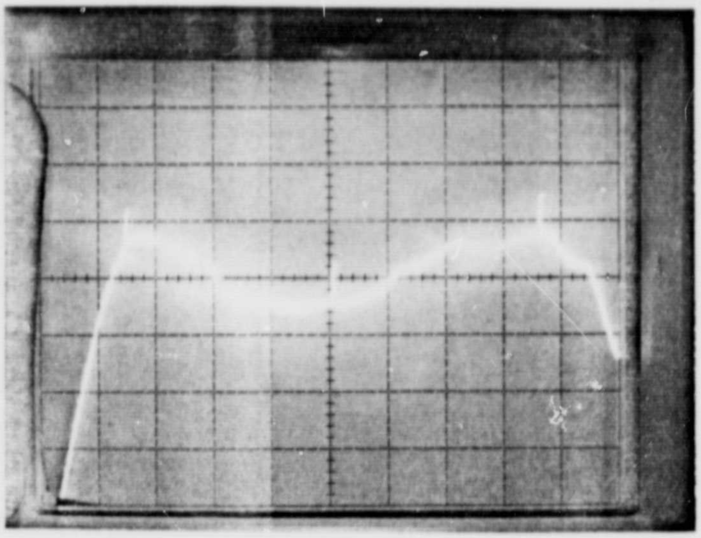
SWITCH AMPLIFIER MODULE
DG7 S/N 010-B
PRE- THERMAL VACUUM TEST
VDS = 5.0 Vdc
VG1 = 0.43 Vdc
VG2 = +0.20 Vdc
Ids = 50 m
Center Gain: 20dB
Markers at 3.5, 4.75 and 6.0 GHz

2 dB/div



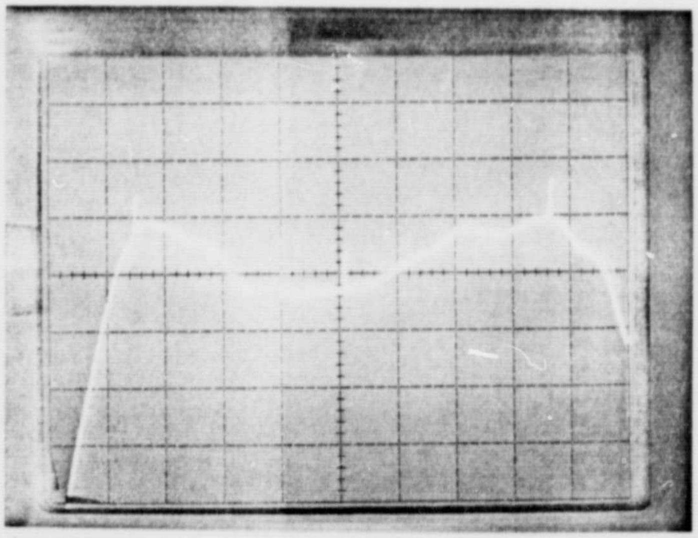
SWITCH AMPLIFIER MODULE
DG7 S/N 010-B
POST -THERMAL-VACUUM TEST
VDS = 5.0 Vdc
VG1 = 0.43 Vdc
VG2 = +0.20 Vdc
Ids = 50 m
Center Gain: 20 dB
Markers at 3.5, 4.75 and 6.0 GH:

2 dB/div

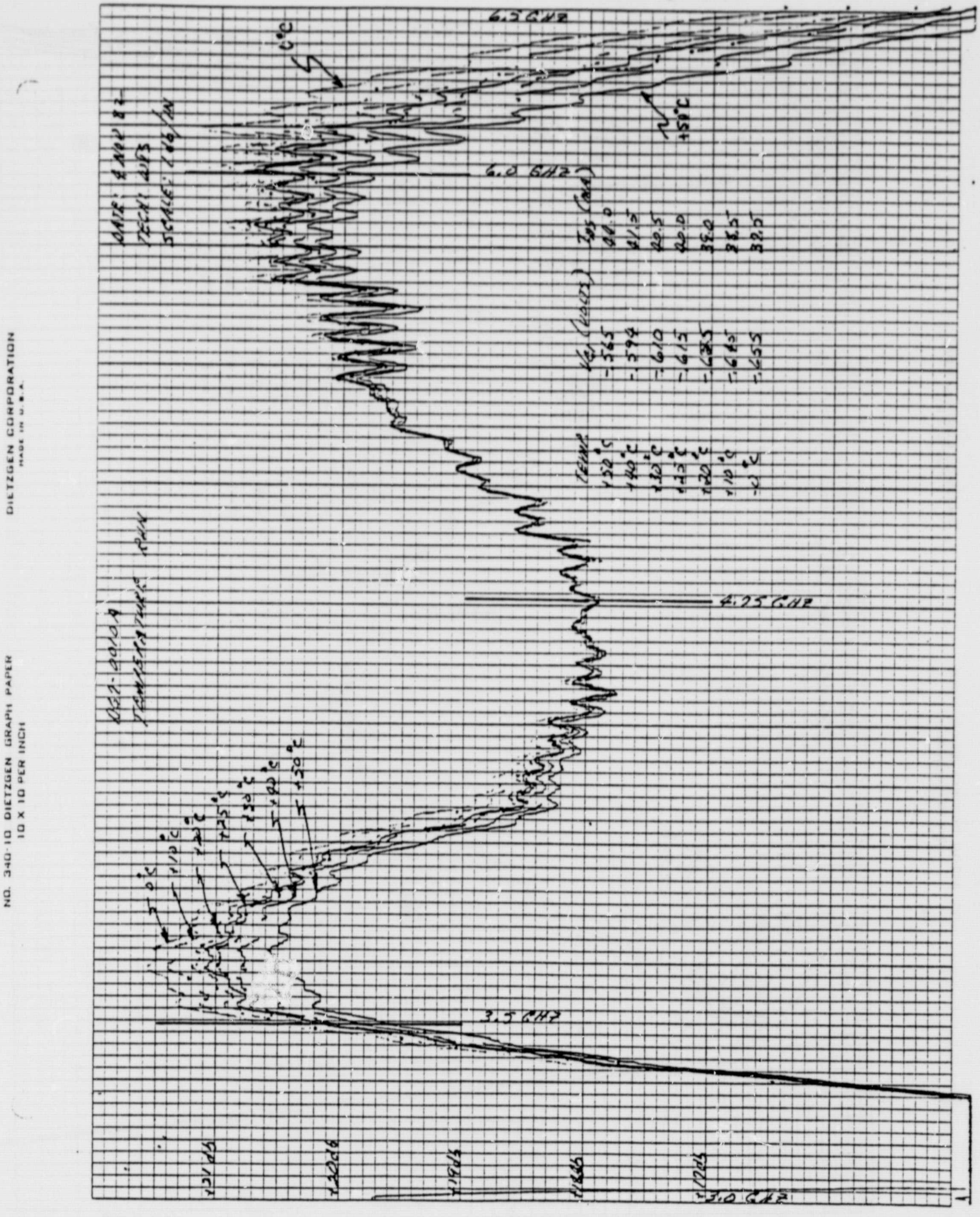


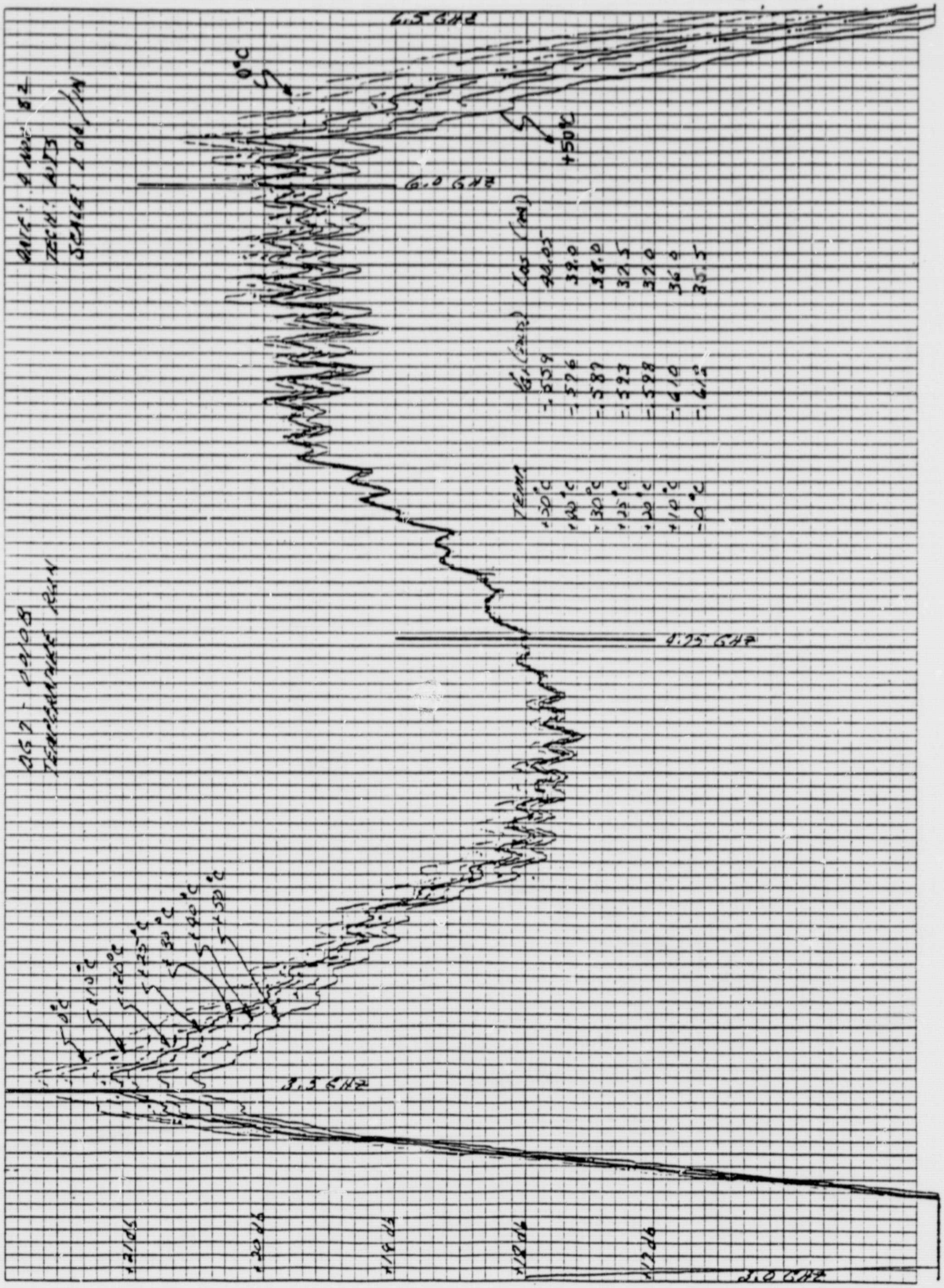
SWITCH AMPLIFIER MODULE
DG7 S/N 010-A
PRE THERMAL VACUUM TEST
VDS = 5.0 Vdc
VG1 = -0.54 Vdc
VG2 = + 0.20 Vdc
Ids = 50 m
Center Gain: 20dB
Markers at 3.5, 4.75 and 6.0 GHz

2 dB/div



SWITCH AMPLIFIER MODULE
DG7 S/N 010-A
POST THERMAL VACUUM TEST
VDS = 5.0 Vdc
VG1 = 0.54 Vdc
VG2 = + 0.20 Vdc
Ids = 50 m
Center Gain: 20dB
MARKERS AT 3.5, 4.75 and 6.0 GHz


6.5 GHz
6.0 GHz
4.25 GHz
3.5 GHz
3.0 GHz


6.5 GHZ
6.0 GHZ
4.75 GHZ
3.5 GHZ
3.0 GHZ

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3.4 Spectrum Analysis Tests

A test was performed on a sample of crosspoints to determine the noise floor characteristics in both the "ON" and "OFF" conditions. To insure that the matrix is stable, a spurious signal search was performed from 0.01 GHz to 22.0 GHz. A sample of crosspoints was tested and typical data is presented.

Additional isolation measurements were also performed using two different frequency signals. This type of test helps to illustrate the differences in isolation that may occur between adjacent and non-adjacent crosspoints.

3.4.1

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #9

NOISE LEVEL TEST

Definition: The noise level is the ratio between the RF signal level and the noise floor level measured at the output port of the matrix for an input power level not higher than 10 dB below the 1-dB compression point.

Test Setup: See Figure 3.4.1.1.

Test Conditions: Frequency: 4750 GHz
Input Power Level: 0 dBm Max.

Test Procedure: Determine on the spectrum analyser screen the noise floor level below the RF carrier level and record data on Table 3.4.1.1. Attach typical photographs.

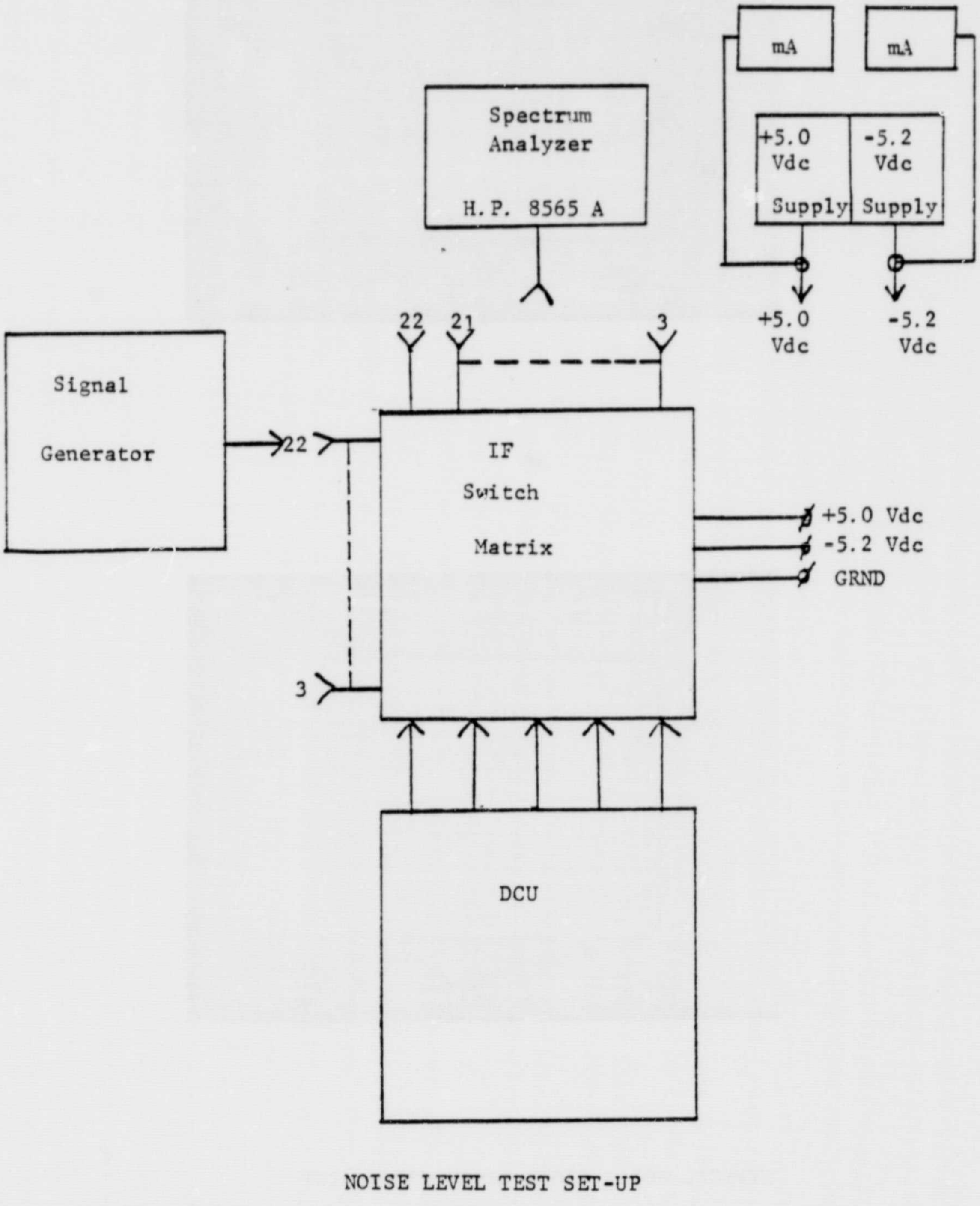
Table 3.4.1.1.

NOISE LEVEL TEST DATA

X- Point #	Input Level dBm	Output Level dBm	Noise Level Below Carrier dBc
6	0.0	-24.0	> 60 dB
31	0.0	-21.3	> 60 dB
37	0.0	-22.6	> 60 dB
66	0.0	-21.7	> 60 dB

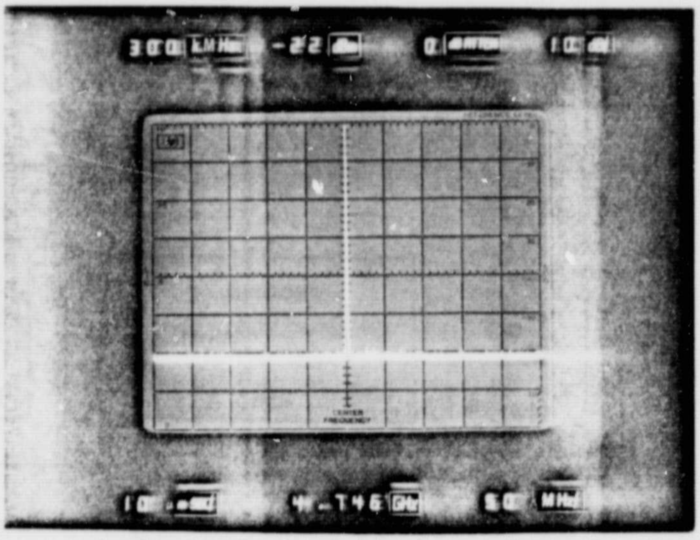
Tested by: A. Anderson
A. Anderson

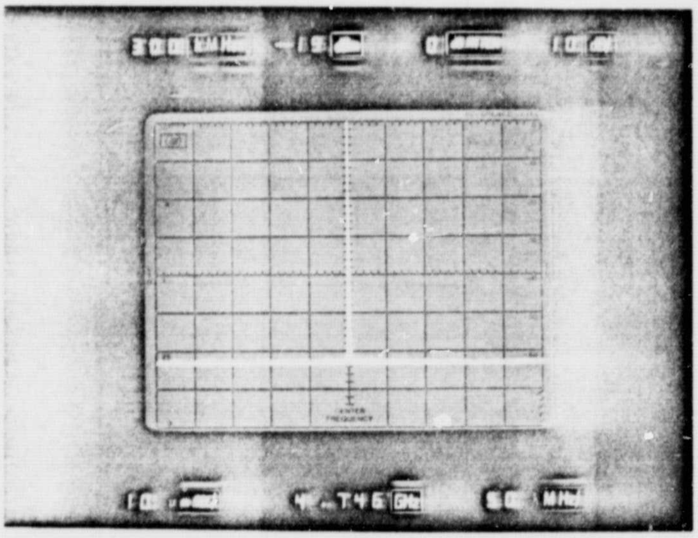
Date: 11/6/1982



NOISE LEVEL TEST SET-UP

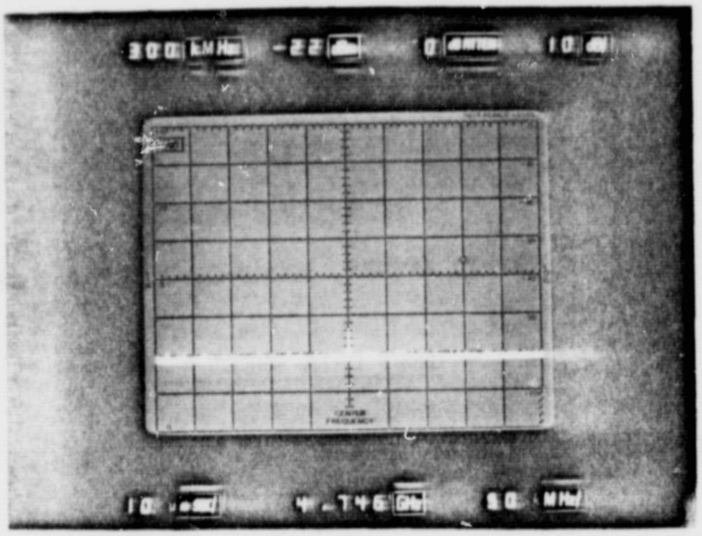
FIGURE 3.4.1.1

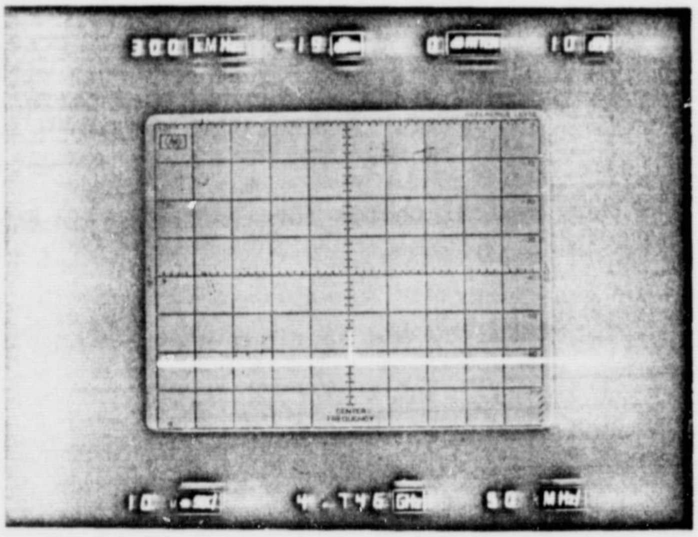




TYPICAL NOISE FLOOR LEVEL CROSSPOINT

SWITCH "ON"





NOISE LEVEL FOR CROSSPOINT SWITCH "OFF"

(Typical)

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3.4.2

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF-OF-CONCEPT MODEL

TEST DATA SHEET #10

STABILITY AND SPURIOUS SIGNALS TEST

Definition: The system is unconditionally stable if no oscillations or non-coherent signals are present at the output ports of the matrix.

Test Setup: See Figure 3.4.2.1.

Test Conditions: Frequency 0.01 Ghz to 22 GHz
Input Lower Level: +10 dBm max.

Test Procedure: The test will be performed by observing the output frequency spectrum of the unit without and with input signal. The test was performed with an HP Spectrum Analyzer. Appropriate bandwidth and sweep rates will be selected to assure adequate sensitivity.

Test Data: Attach typical photos for the tested crosspoints.

Table 3.4.2.1

Stability and spurious signal test

Crosspoint #	6	31	37	66	23	16	45	
Stability	✓	✓	✓	✓	✓	✓	✓	
Spurious	✓	✓	✓	✓	✓	✓	✓	

Tested by: A. Anderson
A.Anderson

Date: 11/6/1982

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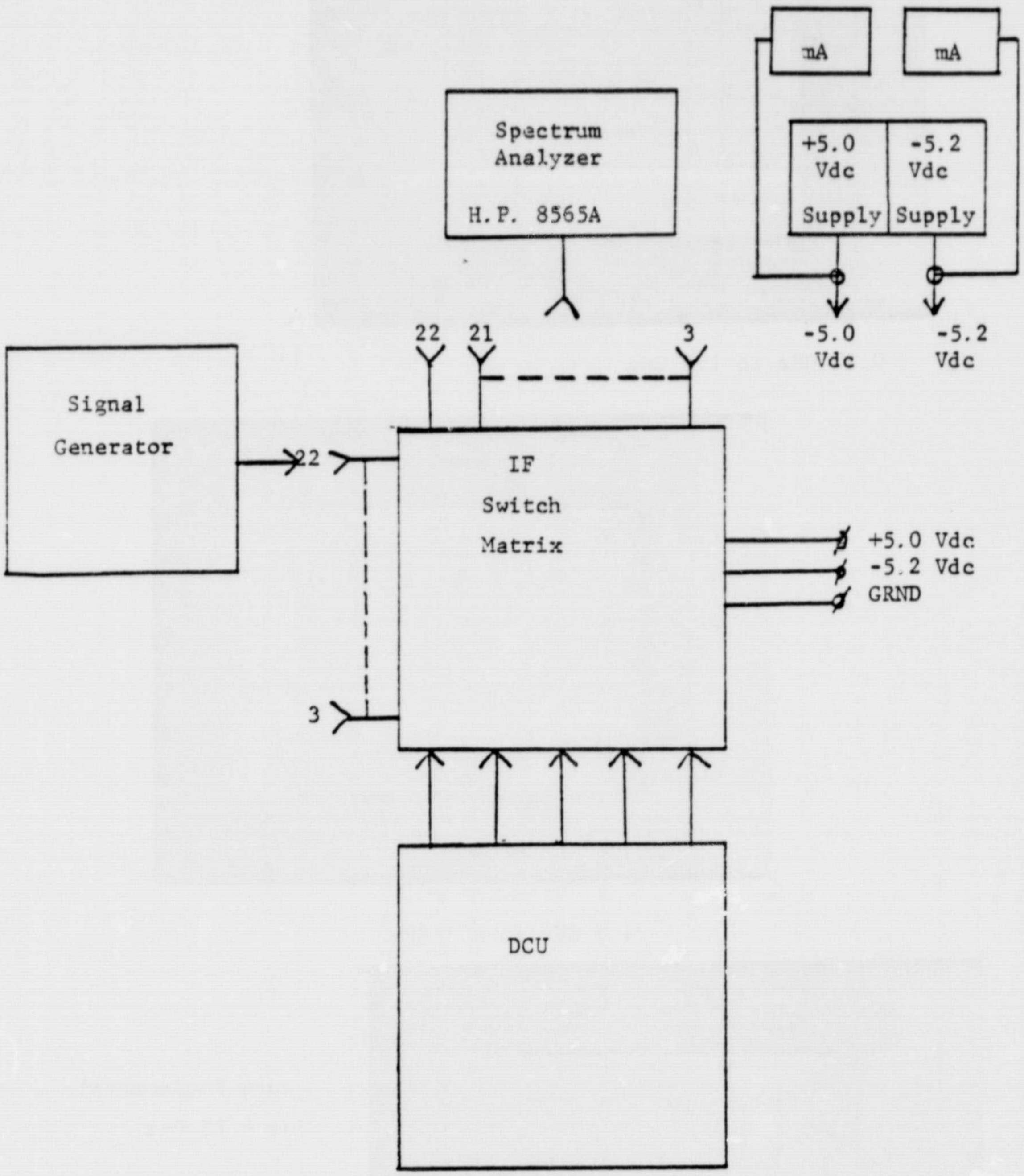
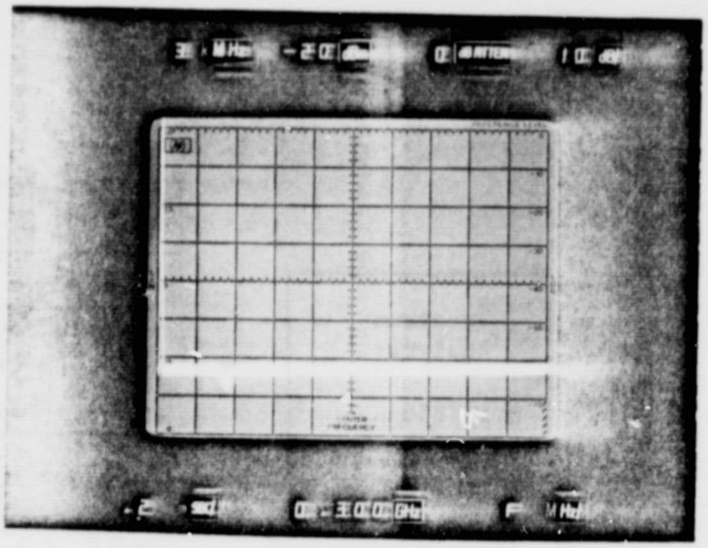
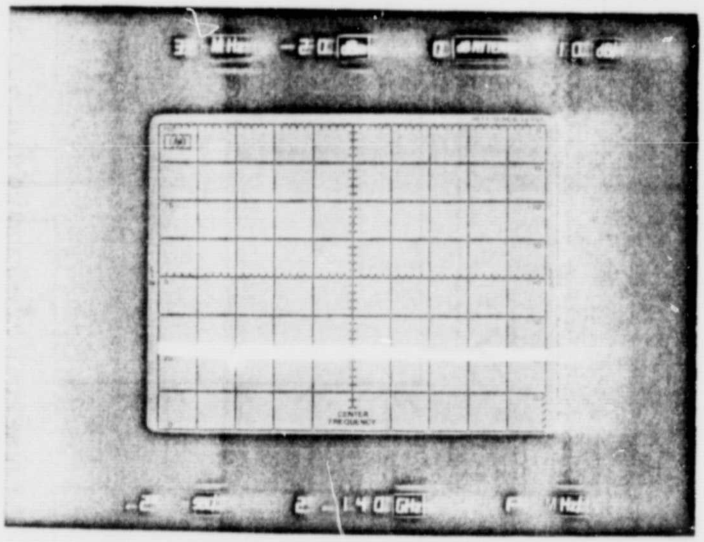


STABILITY AND SPURIOUS SIGNAL TEST SET-UP

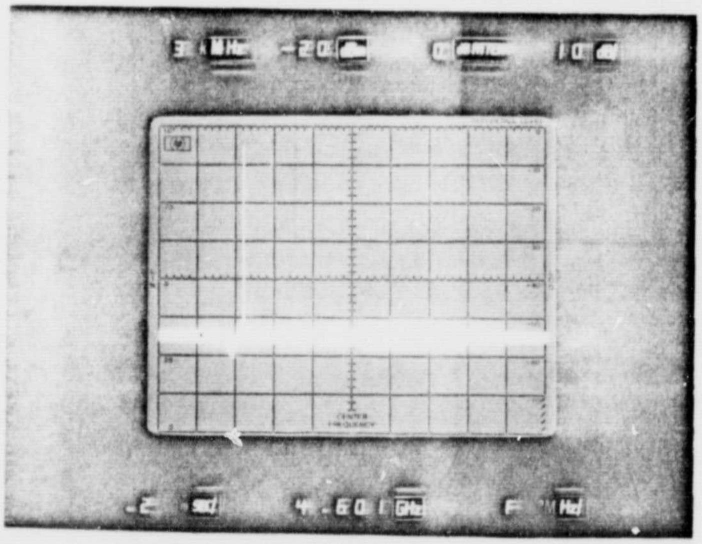
FIGURE 3.4.2.1



0.01 GHz to 1.8 GHz

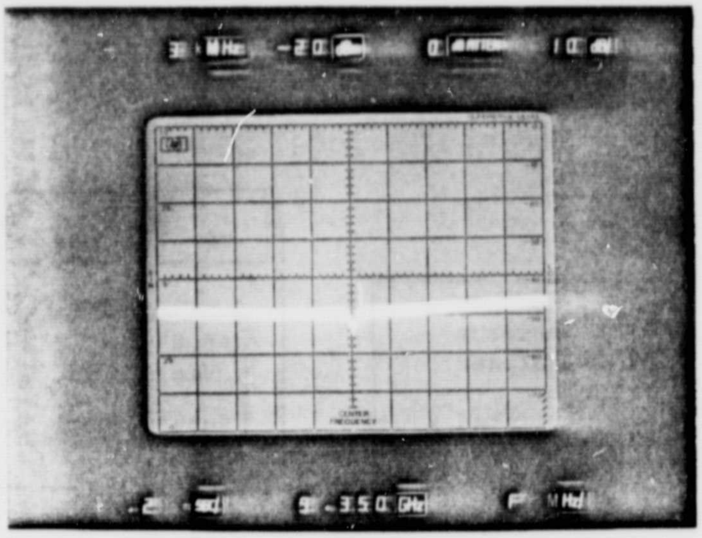


1.7 GHz to 4.1 GHz



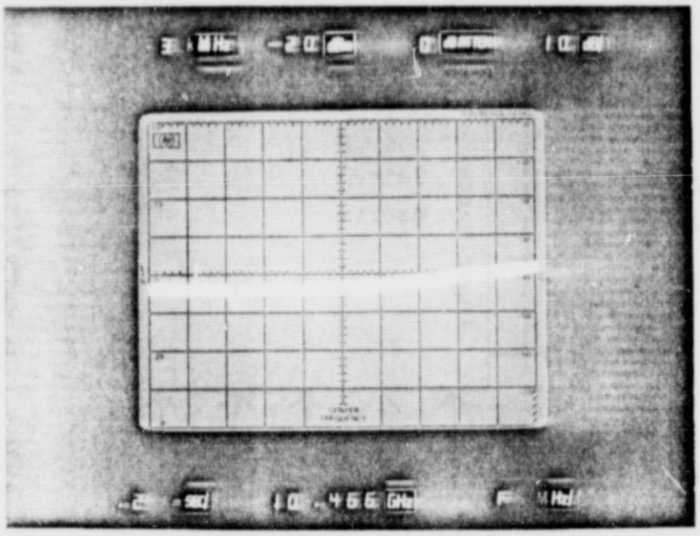
Note Fundamental
at 4.75 GHz

3.8 GHz to 8.5 GHz



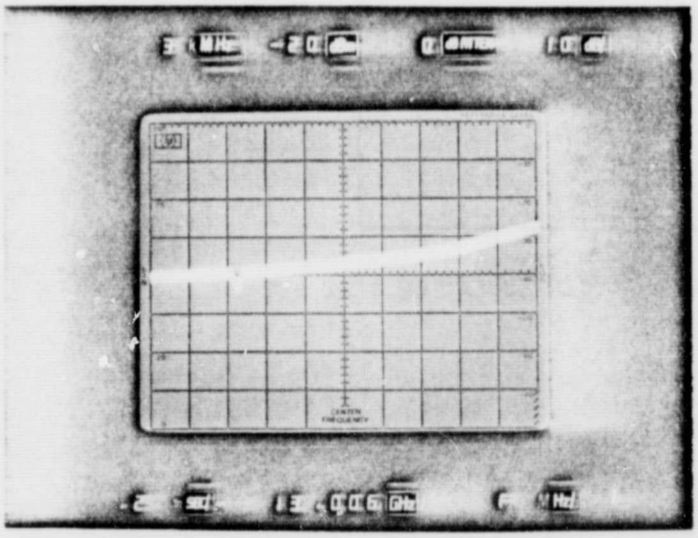
Note Second Harmonic at 9.5 GHz

5.8 GHz to 12.9 GHz



Note Second Harmonic at 9.5 GHz

8.5 GHz to 18.0 GHz



10.5 GHz to 22.0 GHz

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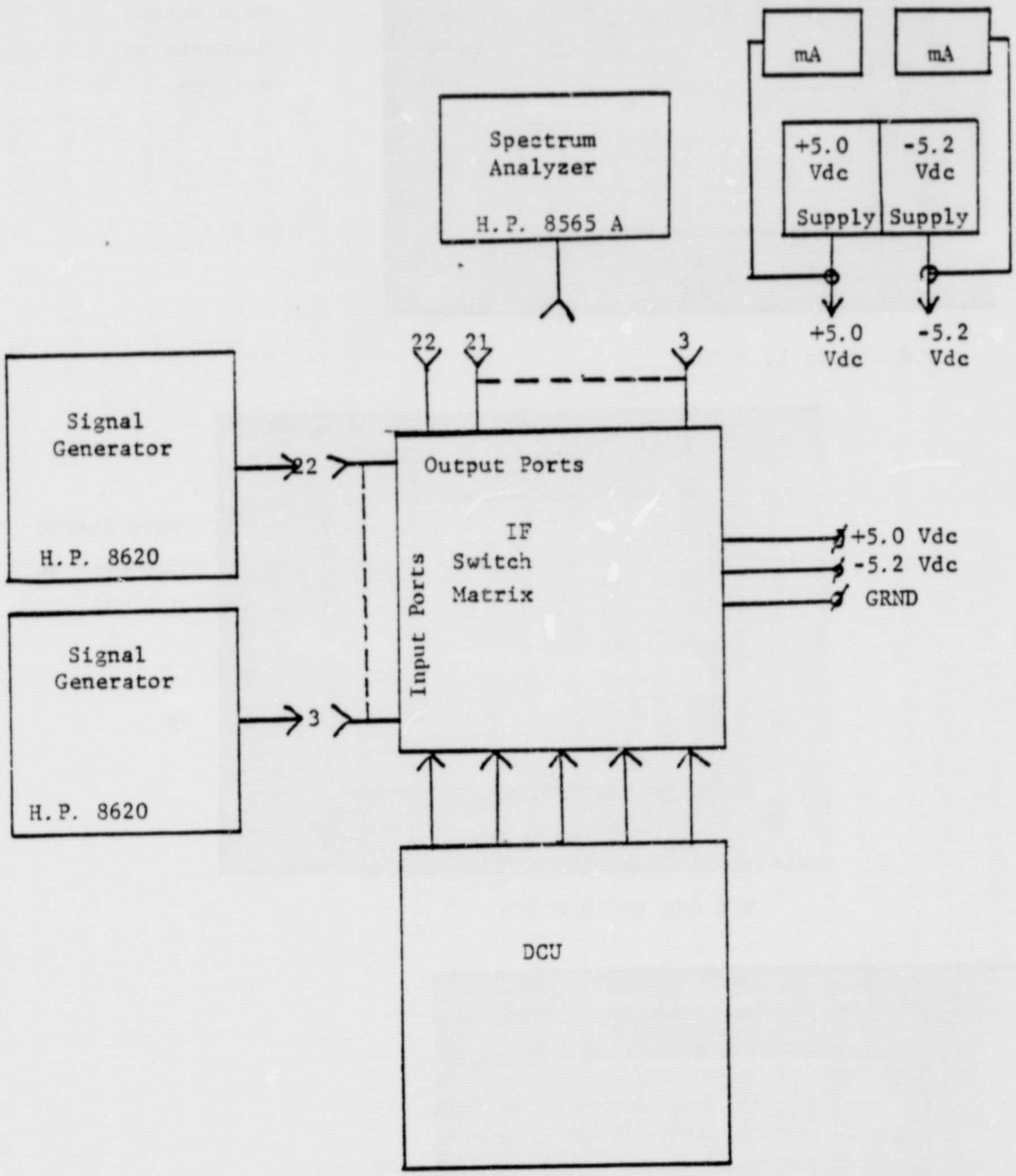
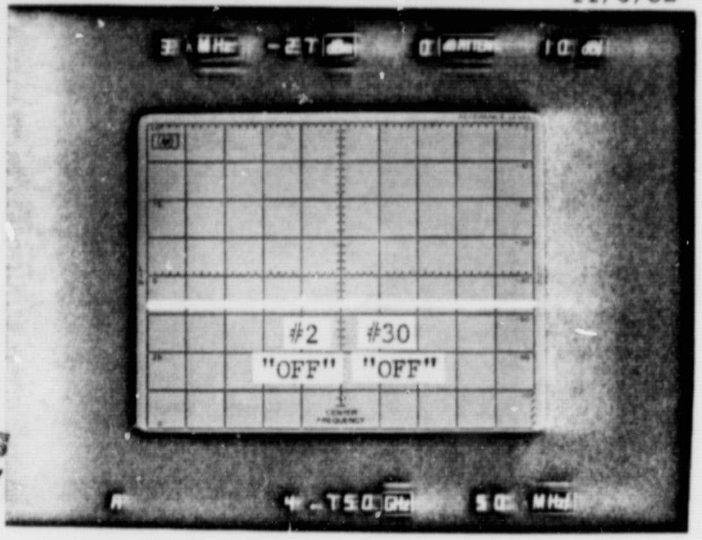
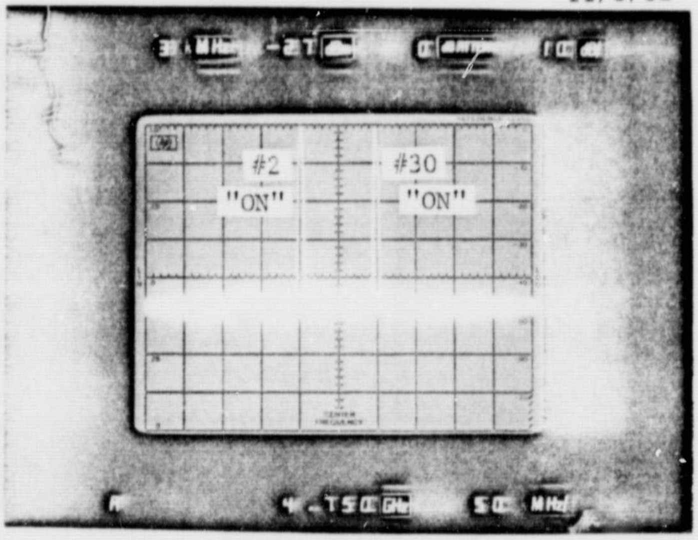


TWO SIGNAL SPECTRUM ANALYZER ISOLATION TEST SET-UP

11/6/82

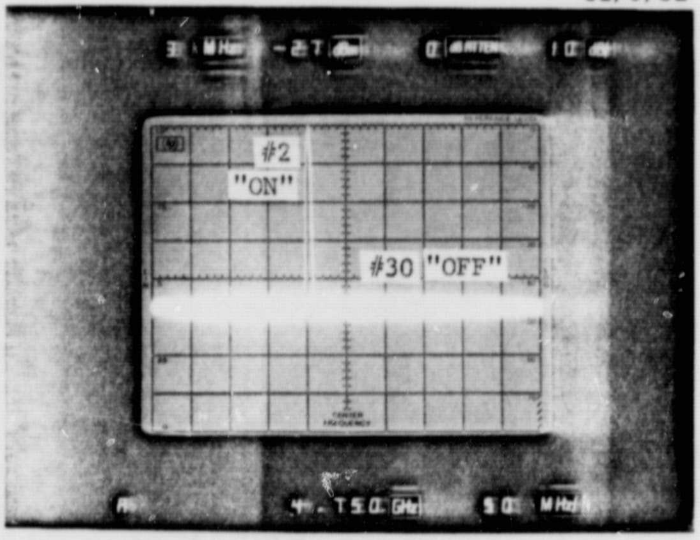


11/6/82

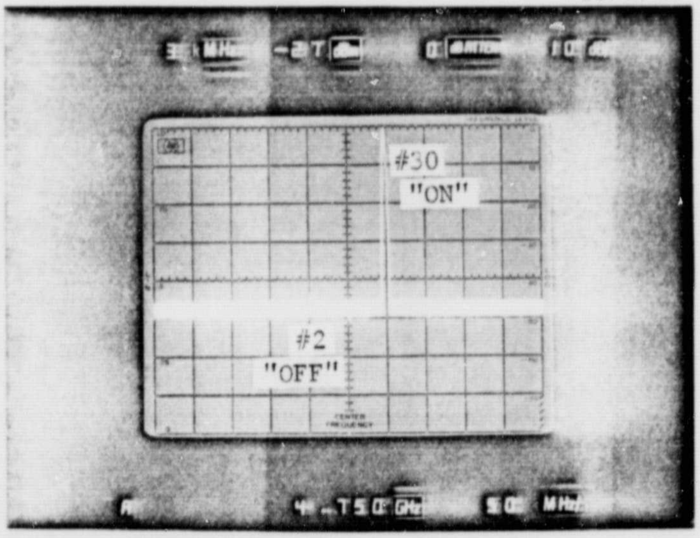


ISOLATION MEASUREMENT CROSSPOINTS #2 AND #30
NON-ADJACENT INPUT PORTS (#'s 4 AND 8)
NON-ADJACENT OUTPUT PORTS (#'6 AND 3)

11/6/82

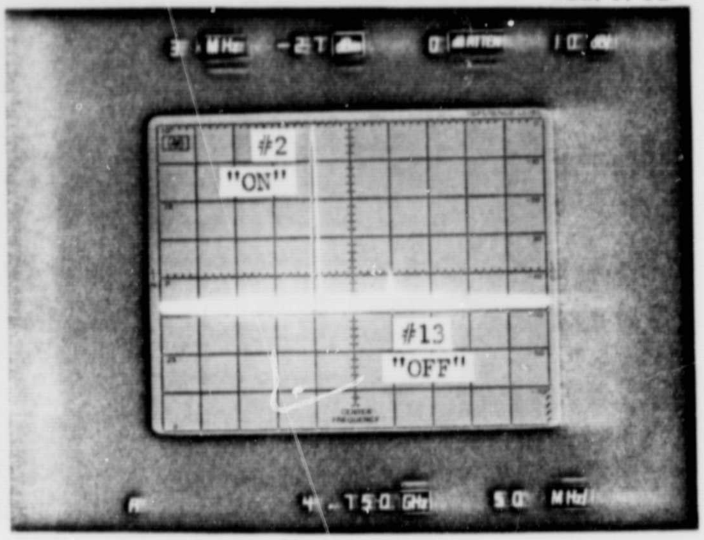


11/6/82

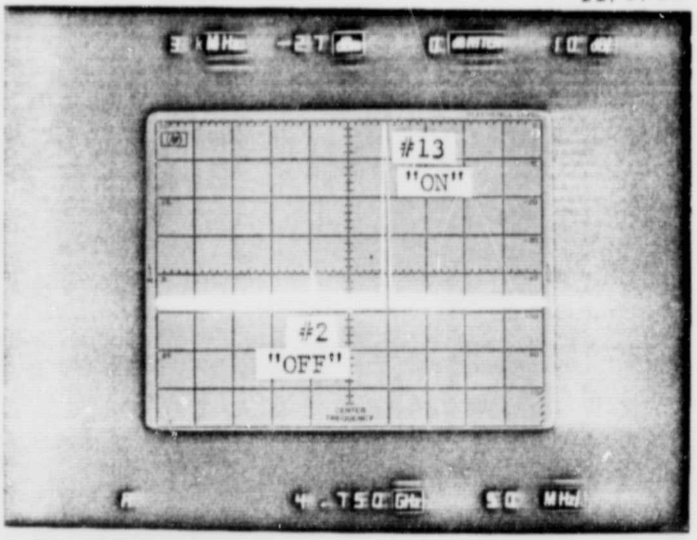


ISOLATION MEASUREMENT CROSSPOINTS #2 AND #30
NON-ADJACENT INPUT PORTS (#'s 4 AND 8)
NON-ADJACENT OUTPUT PORTS (#'s 6 AND 3)

11/6/82



11/6/82



ISOLATION MEASUREMENT CROSSPOINTS #2 AND #13
ADJACENT INPUT PORTS (#'s 3 AND 4)
ADJACENT OUTPUT PORTS (#'s 3 AND 4)

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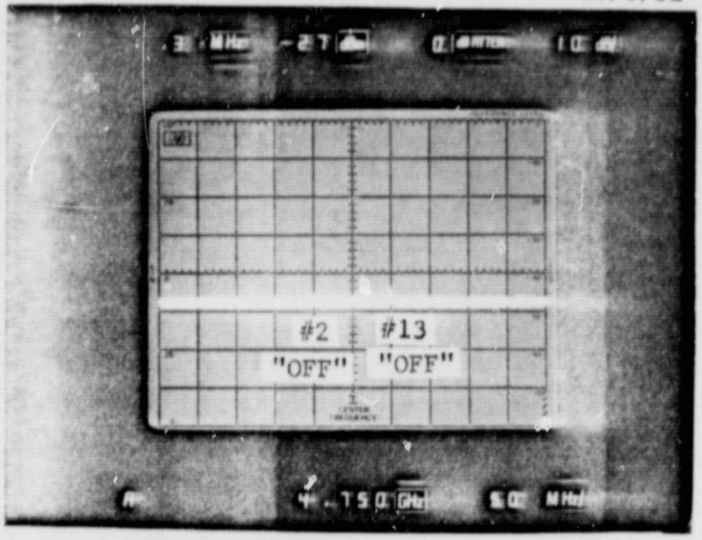
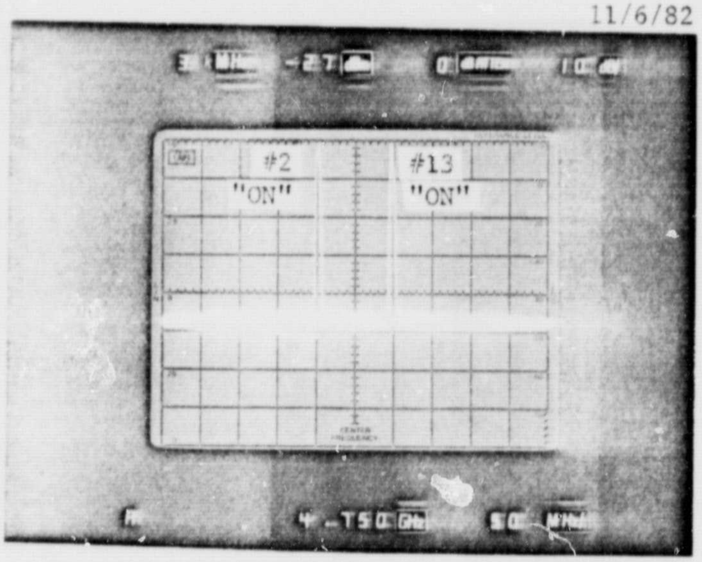


11/6/82



ISOLATION MEASUREMENT CROSSPOINTS #2 AND #13
ADJACENT INPUT PORTS (#'s 3 AND 4)
ADJACENT OUTPUT PORTS (#'s 3 AND 4)

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3.5 Automatic Network Analyzer Tests

Every active crosspoint in the matrix was tested on an Automatic Network Analyzer. The system used the Hewlett-Packard test program - GPM1 and the following parameters were included: "OFF" insertion loss, "ON" insertion loss, input VSWR and Return loss, transmission phase angle, and group delay. A comprehensive statistical summary of the results is also included.

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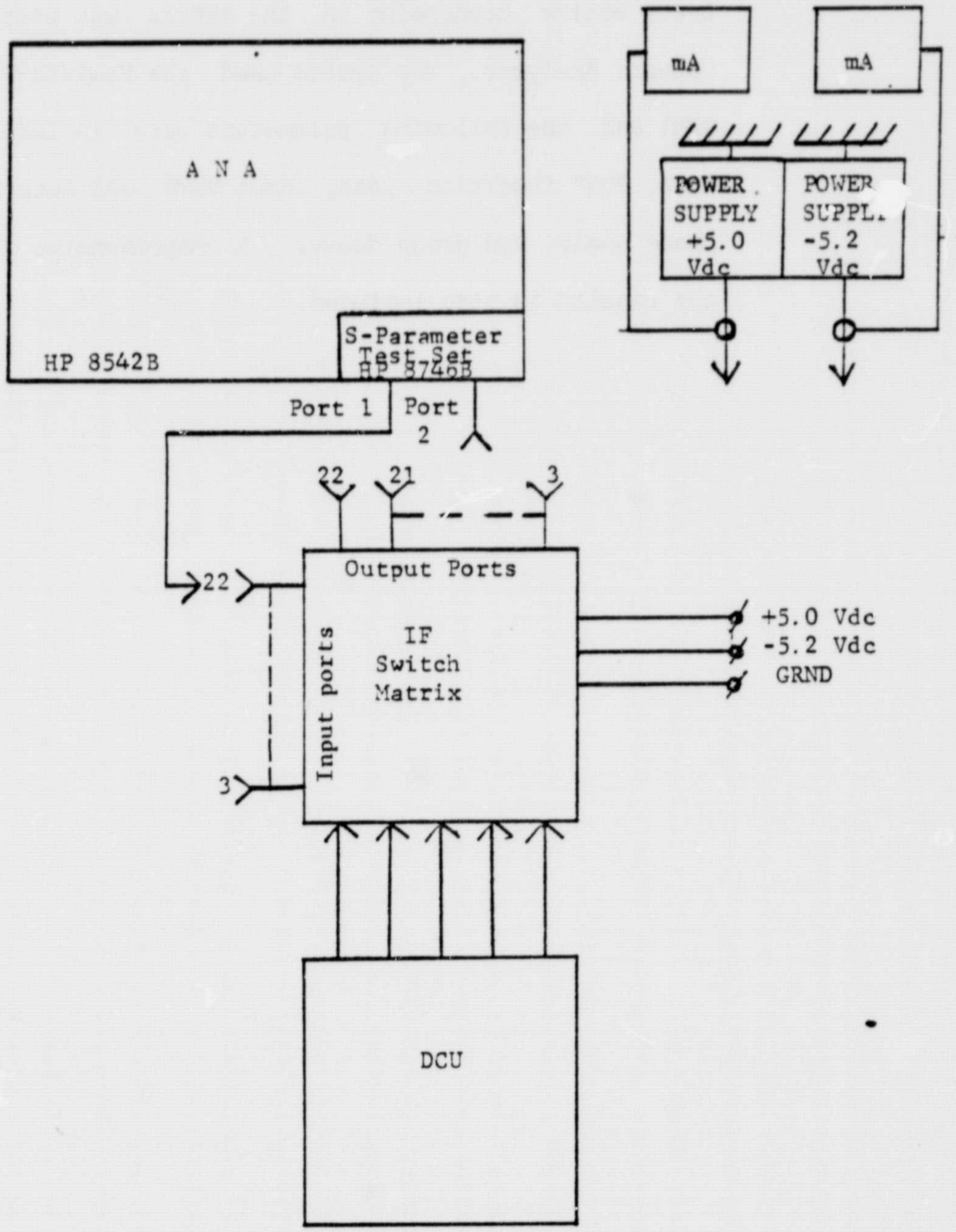

A N A TEST

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3.5.1

ACCEPTANCE TEST

IF SWITCH MATRIX, PROOF OF CONCEPT

TEST DATA SHEET #11

AUTOMATIC NETWORK ANALYSER TEST SUMMARY

4.0 GHZ TO 6.0 GHZ

X-Point #	Isolation (dB)			VSWR			Insertion Loss (dB)		
	$\bar{X}$	S	S^2	X	S	S^2	X	S	S^2
1	77.15	8.28	68.62	1.43	0.26	0.07	20.25	1.62	2.63
2	81.30	5.45	29.75	1.43	0.23	0.05	21.98	1.06	1.12
3	76.94	5.94	35.33	1.37	0.23	0.05	21.42	0.98	0.96
4	77.72	7.75	60.01	1.61	0.41	0.17	21.23	1.18	1.39
5	77.37	5.81	33.74	1.27	0.19	0.04	21.95	0.95	0.91
6	76.39	4.52	20.43	1.52	0.41	0.17	20.54	2.20	4.85
7	74.23	5.51	30.41	1.43	0.27	0.07	21.42	0.75	0.56
8	76.63	5.35	28.67	1.85	0.70	0.49	21.14	0.89	0.79
9	74.01	6.04	36.50	1.51	0.35	0.12	19.22	0.88	0.77
10	74.54	5.37	28.79	1.46	0.33	0.11	22.90	0.74	0.55
11	71.63	4.69	22.01	1.44	0.26	0.07	19.53	0.82	0.68
12	73.24	5.07	25.66	1.59	0.40	0.16	20.05	0.98	0.97
13	76.32	5.41	29.25	1.43	0.27	0.07	22.47	0.85	0.73
14	78.37	6.67	44.44	1.42	0.23	0.05	22.57	1.05	1.10
15	77.39	6.57	43.16	1.37	0.23	0.05	22.43	1.16	1.35
16	76.42	6.69	44.80	1.61	0.41	0.17	22.79	0.74	0.54
17	76.66	6.96	48.40	1.27	0.19	0.04	19.46	0.93	0.87
18	77.96	6.19	38.29	1.53	0.42	0.17	22.11	0.78	0.62
19	75.24	6.37	40.61	1.43	0.27	0.07	20.07	0.84	0.71
20	75.86	5.22	27.30	1.43	0.23	0.05	20.88	1.10	1.22

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X-Point #	Isolation $\bar{X}$	Isolation S	Isolation S^2	VSWR $\bar{X}$	VSWR S	VSWR S^2	Loss $\bar{X}$	Loss S	Loss S^2
21	74.24	5.45	29.69	1.37	0.23	0.05	21.65	0.85	0.72
22	72.18	7.03	49.37	1.61	0.41	0.17	23.02	0.94	0.89
23	69.03	4.88	23.79	1.27	0.19	0.04	19.63	1.91	3.66
24	71.83	3.87	15.01	1.52	0.42	0.17	23.52	1.08	1.17
25	76.34	8.14	66.19	1.43	0.26	0.07	20.01	0.90	0.81
26	77.23	6.04	36.44	1.43	0.23	0.05	20.12	3.31	10.94
27	77.66	7.46	55.69	1.37	0.23	0.05	19.97	1.19	1.41
28	75.86	5.31	28.18	1.61	0.41	0.17	21.59	1.47	2.16
29	76.78	5.62	31.54	1.27	0.19	0.04	22.14	0.83	0.69
30	78.29	5.03	25.29	1.53	0.42	0.17	19.21	1.11	1.24
31	75.80	6.38	40.74	1.43	0.27	0.07	21.21	1.34	1.81
32	77.74	6.18	38.21	1.42	0.22	0.05	22.39	1.22	1.50
33	75.71	6.07	36.81	1.36	0.22	0.05	20.86	1.34	1.79
34	76.62	5.36	28.72	1.61	0.41	0.17	19.43	1.89	3.56
35	78.42	7.46	55.69	1.27	0.19	0.04	19.90	1.51	2.29
36	77.75	5.78	33.42	1.53	0.42	0.17	20.24	1.42	2.02
37	74.02	5.37	28.86	1.43	0.27	0.08	21.84	1.39	1.92
38	75.20	6.17	38.13	1.84	0.68	0.47	20.09	1.28	1.65
39	71.52	5.11	26.13	1.51	0.36	0.13	19.07	0.92	0.85
40	71.70	4.66	21.74	1.46	0.33	0.11	18.91	0.77	0.60

X-Point #	Isolation			VSWR			Loss		
	$\bar{X}$	S	S^2	$\bar{X}$	S	S^2	$\bar{X}$	S	S^2
41	69.26	3.57	12.78	1.44	0.27	0.07	18.07	0.79	0.62
42									
43	72.99	5.73	32.81	1.26	0.19	0.04	19.36	0.91	0.84
44	71.50	5.65	31.87	1.52	0.41	0.17	19.75	0.99	0.98
45	72.94	5.04	25.39	1.43	0.27	0.08	20.27	0.59	0.35
46	71.79	3.98	15.85	1.84	0.69	0.48	18.28	1.00	1.00
47	71.46	8.34	69.49	1.51	0.35	0.12	18.86	0.92	0.85
48	73.23	5.62	31.59	1.46	0.33	0.11	19.40	3.14	9.84
49	67.53	3.86	14.88	1.44	0.26	0.07	19.85	0.81	0.66
50	70.52	5.12	26.22	1.58	0.40	0.16	19.02	1.20	1.44
51	72.88	8.41	70.68	1.26	0.19	0.04	19.87	1.01	1.02
52	73.80	4.38	19.16	1.52	0.41	0.17	20.91	0.78	0.60
53	73.50	5.54	30.69	1.43	0.27	0.07	19.70	0.81	0.66
54	72.29	3.84	14.74	1.84	0.69	0.47	19.36	1.05	1.10
55	71.59	6.64	44.14	1.51	0.35	0.12	18.74	0.91	0.82
56	73.56	6.72	45.22	1.46	0.33	0.11	22.76	1.04	1.07
57	70.11	5.94	35.32	1.44	0.26	0.07	27.58	0.86	0.74
58	72.74	5.88	34.58	1.59	0.40	0.16	19.65	0.89	0.79
59	73.70	7.02	49.21	1.26	0.19	0.04	19.37	1.56	2.43
60	70.81	9.25	85.58	1.52	0.41	0.17	19.70	0.91	0.83

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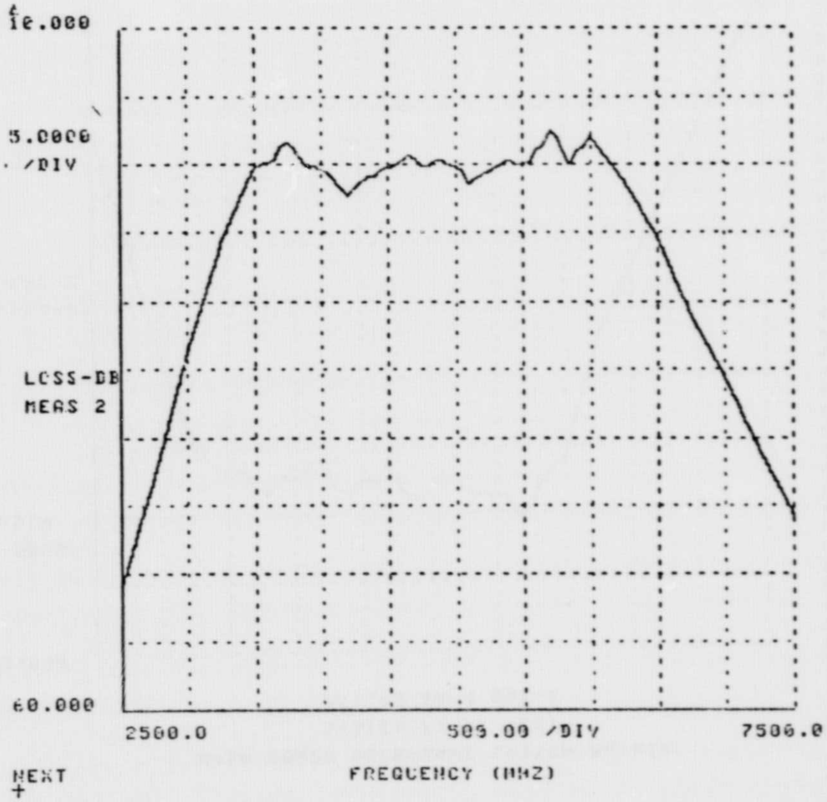
X-Point #	Isolation $\bar{X}$	Isolation S	Isolation S^2	VSWR $\bar{X}$	VSWR S	VSWR S^2	Loss $\bar{X}$	Loss S	Loss S^2
61	75.51	5.79	33.58	1.43	0.27	0.07	19.84	1.26	1.58
62	70.12	7.79	60.72	1.84	0.69	0.48	19.49	1.49	2.22
63	70.61	6.92	47.95	1.49	0.32	0.10	19.26	1.63	2.67
64	71.71	8.53	72.83	1.46	0.32	0.11	20.58	1.33	1.77
65	75.61	6.80	46.19	1.44	0.26	0.07	20.31	1.10	1.21
66	69.49	7.10	50.47	1.58	0.40	0.16	20.31	1.20	1.44

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#1 IN-3 OUT-3



FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	63.50	1.32	17.11	50.96	-24.77	1.27
2750.000	87.32	1.05	31.77	42.95	46.93	3.27
3000.000	90.94	1.42	15.27	33.94	165.74	3.50
3250.000	85.90	1.11	25.96	25.72	137.36	1.76
3500.000	86.25	1.10	26.12	20.27	144.69	1.92
3550.000	94.62	1.39	15.67	20.02	-70.12	11.97
3600.000	78.02	1.51	13.85	19.85	73.82	11.75
3650.000	84.93	1.78	11.02	19.78	-133.20	11.76
3700.000	77.74	1.24	19.42	18.57	10.61	12.05
3750.000	77.21	1.48	14.29	18.42	152.89	12.05
3800.000	71.35	1.23	19.65	16.04	-63.33	11.95
3850.000	76.93	1.44	14.85	19.66	82.70	11.71
3900.000	70.66	1.45	14.70	20.29	-124.70	11.61
3950.000	74.00	1.36	15.92	20.12	24.71	11.71
4000.000	75.71	1.52	13.76	20.42	173.70	11.72
4050.000	72.79	1.44	14.61	20.62	-37.06	11.70
4100.000	72.21	1.15	23.00	21.21	112.60	11.65
4150.000	73.70	1.57	13.07	21.66	-96.40	11.42
4200.000	74.44	1.32	17.12	22.33	61.41	11.32
4250.000	70.69	1.13	24.16	21.74	-143.98	11.51
4300.000	73.23	1.44	14.67	21.30	7.02	11.66
4350.000	73.93	1.47	14.40	20.93	156.23	11.64
4400.000	68.73	1.33	17.09	20.92	-52.10	11.61
4450.000	72.76	1.04	34.42	20.36	98.36	11.71
4500.000	70.72	1.25	19.14	20.27	-113.52	11.70
4550.000	69.96	1.29	17.95	20.06	36.99	11.67
4600.000	70.86	1.49	14.15	19.73	-173.60	11.60
4650.000	67.53	1.49	14.10	19.32	-27.95	11.66
4700.000	66.47	1.35	16.46	19.64	119.42	11.75
4750.000	66.11	1.25	19.16	20.08	-90.88	11.66
4800.000	68.52	1.29	18.07	20.11	55.77	11.64
4850.000	69.50	1.26	18.74	19.74	-149.77	11.73
4900.000	66.26	1.19	21.31	19.60	-2.65	11.85
4950.000	70.60	1.33	17.04	20.03	143.46	11.76
5000.000	70.39	1.44	14.89	20.16	-65.85	11.77
5050.000	68.71	1.32	17.11	20.52	79.67	11.69
5100.000	71.03	1.62	12.56	21.43	-126.59	11.49
5150.000	79.64	1.17	22.03	20.97	26.03	11.60
5200.000	85.76	1.47	14.46	20.76	175.91	11.66
5250.000	85.96	1.52	13.64	20.57	-33.60	11.68
5300.000	79.37	1.25	19.24	20.24	115.46	11.76
5350.000	80.16	1.30	17.79	19.90	-96.85	11.65
5400.000	83.66	1.05	32.66	19.69	48.90	11.66
5450.000	81.73	1.21	20.48	20.01	-163.95	11.73
5500.000	83.75	1.36	16.27	19.98	-13.30	11.67
5550.000	84.90	1.66	12.15	19.87	135.30	11.73
5600.000	82.12	1.45	14.78	18.95	-75.49	11.93
5650.000	83.33	1.36	16.20	18.34	69.69	12.93
5700.000	87.01	1.47	14.37	17.35	-143.57	12.23
5750.000	79.08	1.40	15.61	17.63	-10.33	12.32
5800.000	100.10	1.78	11.04	19.12	131.49	11.77
5850.000	85.55	2.29	9.15	22.01	-73.91	11.61
5900.000	94.01	1.90	10.16	19.06	73.62	11.35
5950.000	88.46	2.18	8.60	18.71	-140.67	12.06
6000.000	83.07	1.92	10.00	17.95	-.64	2.25
6250.000	94.13	1.59	12.34	21.29	-23.59	.11
6500.000	79.39	2.11	8.94	25.37	-30.27	.01
6750.000	73.60	1.37	16.17	31.06	-25.65	1.91
7000.000	80.99	1.31	17.40	35.66	-5.53	1.69
7250.000	75.80	2.91	6.22	40.35	-5.42	.03
7500.000	75.45	1.59	12.81	45.65	-10.54	.03

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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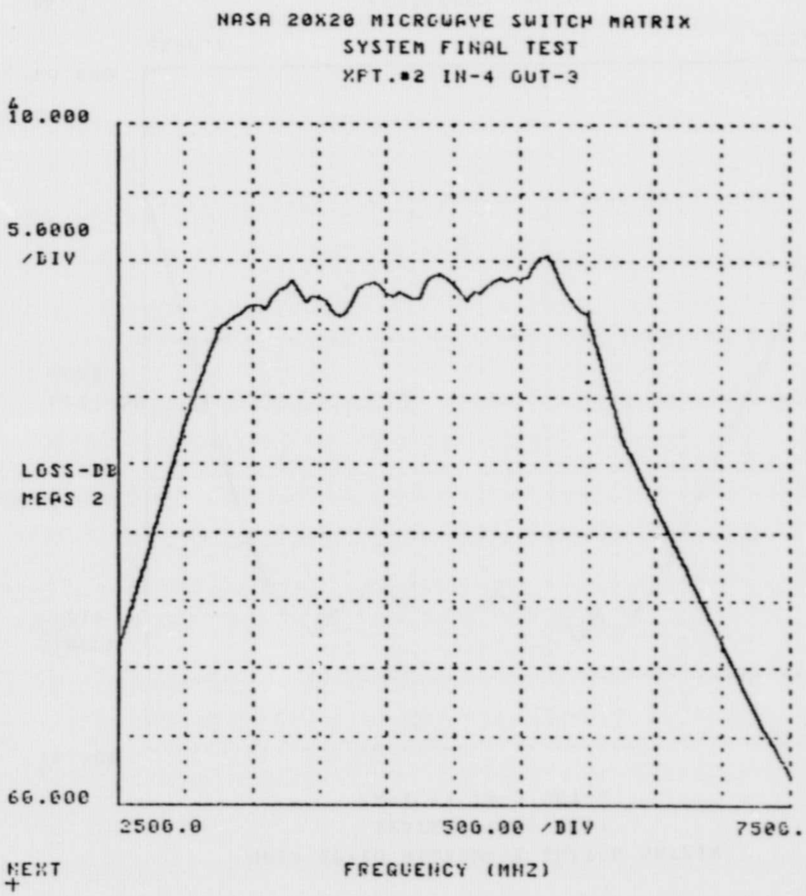

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NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#2 IN-4 OUT-3

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	84.12	1.58	13.01	48.54	-37.67	.52
2750.000	90.45	1.63	12.44	40.62	105.27	2.52
3000.000	91.40	1.15	22.91	32.06	-131.72	2.80
3250.000	86.29	1.16	22.59	24.86	-38.16	3.02
3500.000	82.49	1.47	14.45	23.20	44.71	4.41
3550.000	76.47	1.21	20.50	23.21	-154.11	10.82
3600.000	77.65	1.86	10.41	23.53	15.13	10.69
3650.000	81.65	1.45	14.66	22.70	-175.02	10.94
3700.000	76.45	1.12	24.73	22.14	-18.84	10.96
3750.000	80.62	1.63	12.40	21.94	145.87	10.98
3800.000	86.69	1.16	22.37	21.49	-54.21	11.13
3850.000	83.13	1.35	16.45	22.21	105.29	10.89
3900.000	69.64	1.50	14.02	22.96	-86.09	10.74
3950.000	73.61	1.45	14.73	22.56	76.56	10.85
4000.000	72.37	1.60	12.78	22.72	-116.74	10.90
4050.000	82.45	1.39	15.70	22.90	46.17	10.85
4100.000	74.15	1.51	13.88	23.67	-147.35	10.60
4150.000	79.81	1.48	14.30	23.99	21.51	10.51
4200.000	81.17	1.44	14.92	23.72	-165.82	10.54
4250.000	67.52	1.06	31.24	22.62	2.11	10.83
4300.000	76.51	1.09	27.14	21.85	164.28	11.02
4350.000	83.23	1.08	28.15	21.69	-34.49	11.02
4400.000	67.26	1.07	28.88	21.45	127.56	11.02
4450.000	79.74	1.22	20.03	21.76	-71.11	10.94
4500.000	77.20	1.27	18.41	22.34	93.85	10.78
4550.000	87.65	1.29	18.05	22.60	-99.31	10.77
4600.000	75.42	1.30	17.60	22.27	66.26	10.81
4650.000	81.33	1.62	12.54	22.51	-128.54	10.83
4700.000	76.17	1.45	14.76	22.76	36.39	10.64
4750.000	73.49	1.59	12.81	22.70	-151.48	10.67
4800.000	83.95	1.39	15.80	21.42	12.36	10.99
4850.000	80.15	1.22	20.19	21.09	172.95	11.06
4900.000	87.08	1.23	19.73	20.95	-25.76	11.09
4950.000	78.08	1.30	17.65	21.18	133.70	11.05
5000.000	80.96	1.56	12.99	21.64	-63.48	10.93
5050.000	75.20	1.60	10.88	22.15	100.13	10.62
5100.000	74.45	1.52	13.68	22.82	-93.10	10.66
5150.000	86.55	1.65	12.17	22.17	75.64	10.[illegible]
5200.000	93.22	1.55	13.32	22.28	-122.32	10.91
5250.000	80.34	1.04	34.66	21.60	42.76	10.85
5300.000	87.63	1.27	18.49	21.45	-152.92	11.03
5350.000	83.75	1.30	17.74	21.20	5.53	11.08
5400.000	81.53	1.49	14.09	21.46	160.27	10.99
5450.000	65.50	1.27	18.45	21.17	-30.16	11.00
5500.000	76.44	1.23	19.87	21.28	132.26	10.95
5550.000	60.12	1.48	14.22	21.16	-65.71	10.96
5600.000	79.09	1.75	11.28	20.32	97.62	11.18
5650.000	80.76	1.20	21.00	19.75	-108.10	11.45
5700.000	84.48	1.45	14.71	19.63	45.33	11.51
5750.000	90.82	1.65	12.23	20.38	-162.44	11.39
5800.000	86.69	1.85	10.48	21.52	-4.76	11.20
5850.000	89.48	1.71	11.54	22.44	154.35	11.13
5900.000	63.04	1.78	11.38	23.10	-45.65	11.15
5950.000	80.23	1.86	10.41	23.61	113.10	11.33
6000.000	85.66	1.45	14.70	23.80	-93.44	4.48
6250.000	74.61	1.57	13.10	33.01	-10.32	2.99
6500.000	79.00	1.98	9.65	37.98	37.99	2.91
6750.000	80.30	1.31	17.34	43.08	-173.23	2.85
7000.000	75.48	1.53	13.54	48.28	-65.07	2.83
7250.000	73.21	1.54	13.43	53.43	39.03	2.89
7500.000	76.73	1.83	10.57	57.35	133.37	.39

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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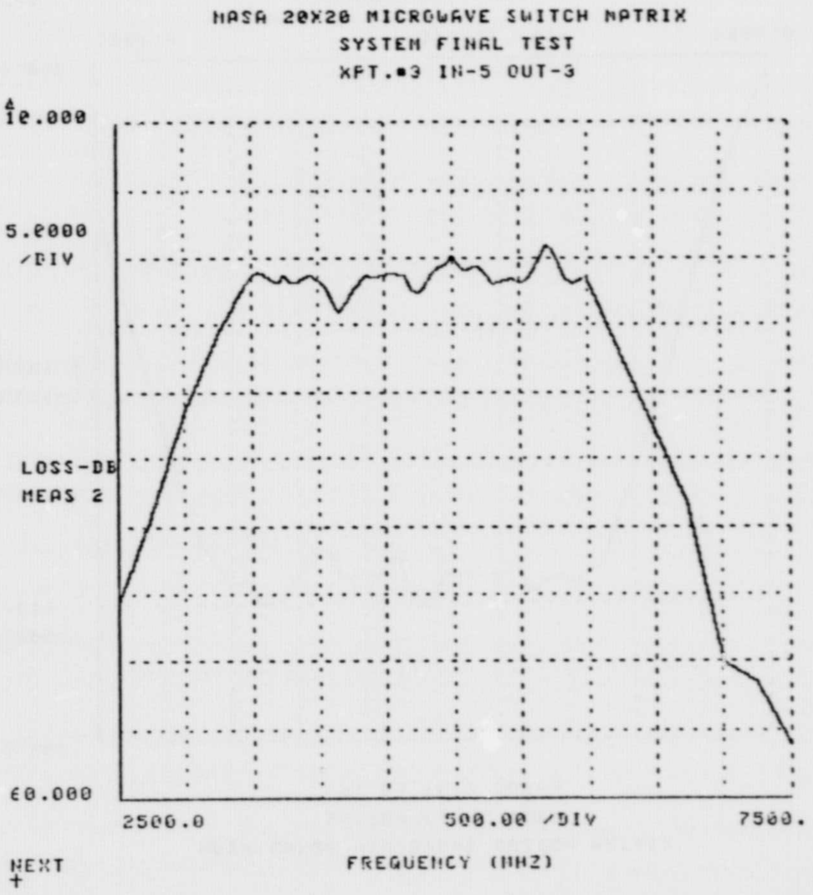

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XFT.#3 IN-5 OUT-3

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	82.92	1.29	18.02	45.60	137.64	.68
2750.000	87.05	1.09	27.17	39.21	-96.52	2.68
3000.000	86.87	1.26	18.91	31.62	14.00	2.87
3250.000	86.90	1.14	23.86	25.67	106.56	3.12
3500.000	79.20	1.08	28.75	21.32	172.47	4.61
3550.000	87.27	1.17	22.01	21.10	-30.93	11.26
3600.000	75.91	1.31	17.35	21.23	126.37	11.16
3650.000	82.28	1.90	10.19	21.59	-72.61	11.10
3700.000	74.86	2.11	8.96	21.64	86.66	10.99
3750.000	72.91	1.36	15.98	21.27	-108.38	11.68
3800.000	75.25	1.41	15.45	21.84	47.90	11.03
3850.000	79.61	1.34	16.72	21.76	-145.55	10.92
3900.000	70.95	1.02	38.92	21.43	14.64	11.15
3950.000	74.14	1.14	23.43	21.28	172.91	11.17
4000.000	71.00	1.13	24.05	21.67	-27.64	11.13
4050.000	76.70	1.20	20.96	22.02	132.17	11.09
4100.000	71.05	1.19	21.07	22.98	-66.98	10.80
4150.000	73.12	1.36	16.37	23.90	100.60	10.56
4200.000	61.53	1.59	12.80	23.51	-87.15	10.68
4250.000	74.40	1.17	22.18	22.60	76.20	10.98
4300.000	70.22	1.14	23.53	22.01	-122.54	11.12
4350.000	72.32	1.14	23.90	21.34	37.02	11.16
4400.000	64.08	1.17	22.11	21.40	-164.13	11.09
4450.000	76.80	1.27	18.62	21.39	-3.64	11.04
4500.000	77.99	1.38	15.90	21.25	158.51	11.11
4550.000	80.64	1.26	18.64	21.12	-42.86	11.15
4600.000	71.31	1.23	19.75	21.25	117.24	11.14
4650.000	73.47	1.20	20.86	21.29	-83.74	11.11
4700.000	70.28	1.39	15.75	22.35	77.27	10.87
4750.000	74.61	1.27	18.47	22.65	-114.94	10.71
4800.000	75.26	1.58	12.91	22.07	51.74	10.80
4850.000	72.82	1.64	12.34	21.19	-146.63	11.09
4900.000	70.91	1.59	12.90	20.77	12.45	11.18
4950.000	82.82	1.57	13.69	20.49	176.89	11.23
5000.000	75.71	1.32	17.12	19.82	-31.80	11.36
5050.000	73.61	1.26	18.86	20.54	122.04	11.21
5100.000	73.63	1.25	19.23	20.92	-75.24	11.03
5150.000	79.45	1.31	17.56	20.66	85.13	11.21
5200.000	73.93	1.09	27.63	20.67	-116.65	11.30
5250.000	76.34	1.20	20.93	21.17	30.25	11.09
5300.000	74.57	1.46	14.50	21.89	-157.76	10.97
5350.000	79.10	1.09	27.16	21.85	3.35	11.05
5400.000	79.71	1.22	20.19	21.63	164.35	11.13
5450.000	91.34	1.25	19.20	21.61	-37.31	11.14
5500.000	80.36	1.26	18.86	21.87	123.14	11.05
5550.000	82.[illegible]	1.55	13.37	21.72	-74.97	11.02
5600.000	78.[illegible]	1.39	15.71	20.95	36.53	11.16
5650.000	72.60	1.21	20.44	20.00	-116.73	11.59
5700.000	93.06	1.27	18.55	19.02	32.54	11.73
5750.000	73.65	1.42	15.19	19.47	-178.93	11.63
5800.000	79.14	1.63	12.46	20.57	-27.81	11.34
5850.000	90.79	1.94	9.87	21.61	132.57	11.16
5900.000	80.46	1.08	16.32	21.96	-70.27	11.22
5950.000	82.91	1.99	9.60	21.67	98.98	11.48
6000.000	82.14	1.55	13.22	21.42	-123.39	4.81
6250.000	78.69	1.50	14.03	27.20	-70.39	3.39
6500.000	74.25	2.22	8.41	32.80	-14.47	3.37
6750.000	76.59	1.47	14.45	38.55	43.69	3.15
7000.000	68.75	1.77	11.15	50.01	139.67	3.07
7250.000	70.59	1.79	10.96	51.47	-148.57	3.12
7500.000	78.19	2.30	8.07	56.12	-63.09	1.12

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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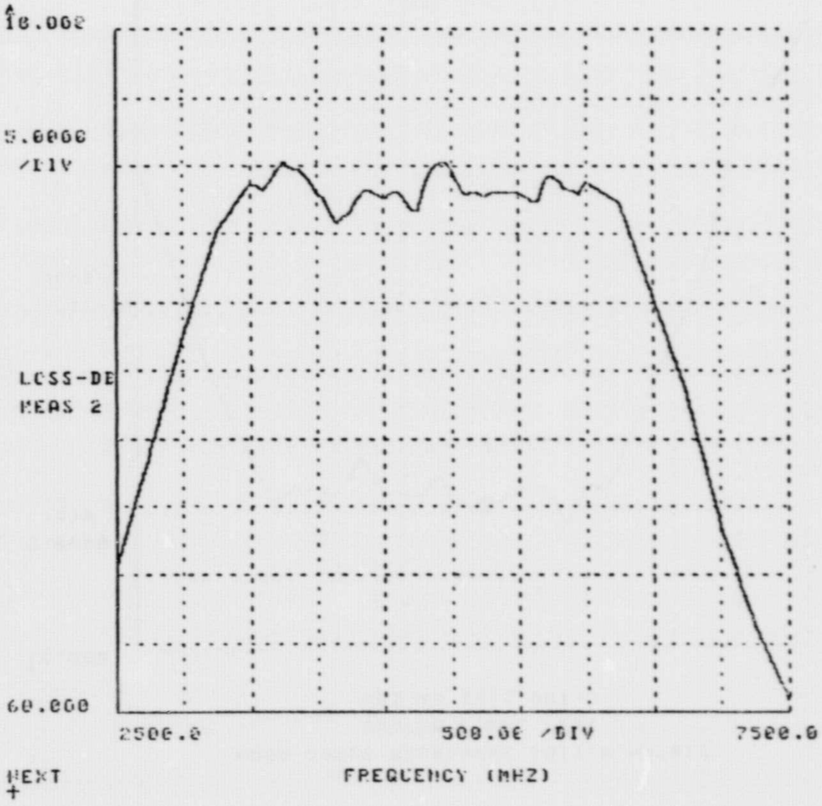
NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#5 IN-7 OUT-3

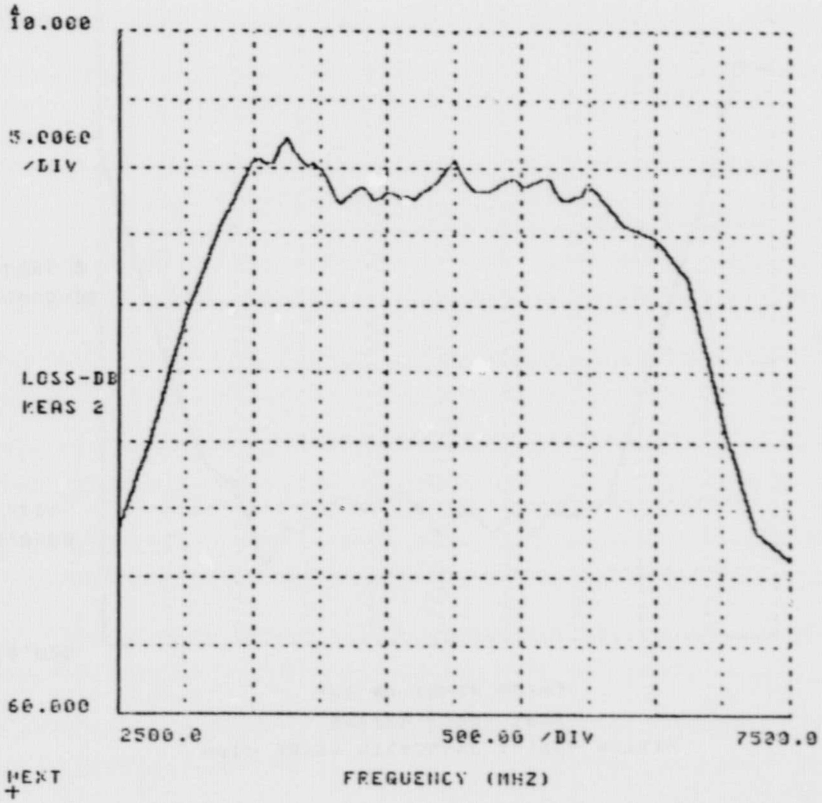


NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#5 IN-7 OUT-3

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	88.78	1.14	23.41	49.33	-4.66	.10
2750.000	81.41	1.52	13.66	41.06	174.09	2.10
3000.000	89.04	1.11	25.79	32.52	-22.56	2.35
3250.000	88.67	1.13	24.58	24.77	110.59	2.63
3500.000	91.26	1.25	19.15	21.35	-136.53	4.65
3550.000	78.16	1.13	24.21	21.47	33.06	10.49
3600.000	72.20	1.33	17.06	21.00	-154.17	10.34
3650.000	75.03	1.42	15.19	21.22	20.71	10.44
3700.000	68.96	1.43	15.02	20.36	-170.17	10.67
3750.000	77.62	1.69	26.90	19.72	-3.42	10.75
3800.000	78.27	1.33	17.03	20.16	162.69	10.65
3850.000	76.62	1.56	13.99	20.20	-26.85	10.61
3900.000	74.34	1.34	16.75	20.58	140.65	10.66
3950.000	74.06	1.30	17.81	21.13	-50.57	16.52
4000.000	63.73	1.30	17.77	21.96	121.04	10.41
4050.000	73.25	1.15	22.90	22.36	-65.25	10.41
4100.000	79.64	1.24	19.27	23.36	106.94	10.24
4150.000	83.93	1.12	25.22	24.15	-73.90	10.00
4200.000	72.06	1.28	16.14	23.65	166.91	10.11
4250.000	79.72	1.20	18.15	23.30	-78.00	10.20
4300.000	80.13	1.12	24.90	22.42	96.76	10.45
4350.000	69.49	1.13	24.11	21.68	-94.24	10.58
4400.000	65.23	1.17	22.18	21.86	76.06	10.56
4450.000	73.73	1.25	19.05	22.10	-112.10	10.36
4500.000	65.01	1.28	18.20	22.36	62.22	10.35
4550.000	73.33	1.14	23.45	22.05	-124.80	19.46
4600.000	70.52	1.11	25.59	21.69	45.49	10.51
4650.000	80.09	1.21	20.54	22.35	-143.15	10.42
4700.000	77.41	1.10	26.44	23.13	30.53	10.06
4750.000	76.07	1.35	16.60	23.31	-145.37	10.00
4800.000	81.62	1.13	23.96	21.52	36.49	10.44
4850.000	73.85	1.06	30.06	20.35	-161.13	10.71
4900.000	72.05	1.10	26.39	19.82	4.63	10.82
4950.000	65.51	1.32	17.22	19.73	169.10	10.83
5000.000	79.47	1.17	22.18	20.23	-25.22	10.68
5050.000	69.61	1.23	19.82	21.26	144.62	10.46
5100.000	73.51	1.16	22.64	22.12	-41.85	10.29
5150.000	92.28	1.17	22.18	22.00	134.25	10.37
5200.000	79.32	1.27	18.55	21.98	-55.01	10.49
5250.000	81.43	1.18	21.52	22.22	116.66	10.36
5300.000	73.40	1.17	22.08	21.97	-67.65	10.46
5350.000	79.65	1.35	16.48	21.93	100.07	10.59
5400.000	75.56	1.27	18.57	21.90	-88.93	10.51
5450.000	72.21	1.44	14.64	21.99	61.09	10.52
5500.000	73.77	1.35	16.51	22.00	-107.63	10.59
5550.000	75.02	1.31	17.33	22.21	60.79	10.52
5600.000	76.70	1.10	26.73	22.55	-126.47	10.30
5650.000	74.16	1.32	17.31	22.39	50.16	10.39
5700.000	76.42	1.11	25.64	20.36	-140.56	10.70
5750.000	83.97	1.11	25.57	20.73	22.03	10.92
5800.000	72.62	1.32	17.17	21.13	-173.79	10.74
5850.000	77.22	1.71	11.60	21.73	-4.44	10.60
5900.000	72.73	1.73	11.45	21.81	164.73	10.56
5950.000	83.97	1.97	9.73	22.06	-24.58	10.65
6000.000	87.43	1.61	12.60	21.21	141.56	4.33
6250.000	69.57	1.04	34.46	22.67	-121.94	2.92
6500.000	79.49	1.20	20.86	29.61	-24.50	2.75
6750.000	69.96	1.23	19.67	36.67	103.62	2.50
7000.000	67.03	1.58	12.91	46.51	-113.69	2.49
7250.000	72.34	1.14	23.61	53.63	15.29	2.25
7500.000	69.57	1.30	17.77	59.15	-156.79	.23

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#7 IN-11 OUT-3



10-28-82

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#7 IN-11 OUT-3

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	62.30	1.14	23.57	46.54	16.00	1.66
2750.000	78.61	1.01	43.71	35.55	-127.59	1.66
3000.000	81.57	1.37	16.16	30.95	74.54	1.92
3250.000	68.97	1.15	23.19	24.39	-113.35	2.14
3500.000	72.23	1.27	18.47	19.45	49.70	3.57
3550.000	82.74	1.28	18.16	19.39	-136.91	10.26
3600.000	80.45	1.10	26.21	19.70	40.22	9.98
3650.000	79.03	1.62	12.56	19.55	-136.15	10.05
3700.000	65.19	1.62	12.55	16.39	38.46	10.32
3750.000	79.65	1.20	20.80	17.76	-149.50	10.44
3800.000	76.23	1.14	23.47	18.69	22.49	10.27
3850.000	69.30	1.23	19.72	19.32	-159.13	10.01
3900.000	79.13	1.25	19.09	19.80	22.03	10.03
3950.000	77.93	1.08	28.75	19.66	-160.15	10.14
4000.000	74.23	1.11	25.71	20.03	17.02	10.14
4050.000	72.21	1.08	28.02	20.75	-165.27	10.04
4100.000	74.34	1.23	19.68	21.91	15.44	9.79
4150.000	71.96	1.05	32.69	22.61	-157.76	9.60
4200.000	76.27	1.38	15.85	22.10	29.81	9.81
4250.000	65.17	1.24	19.54	21.60	-150.97	10.20
4300.000	60.69	1.15	22.66	21.37	29.93	10.09
4350.000	72.74	1.06	31.15	21.58	-154.33	10.05
4400.000	74.34	1.39	15.80	22.37	26.31	9.79
4450.000	64.76	1.50	13.99	22.19	-146.59	9.83
4500.000	77.36	1.26	18.74	21.77	34.26	10.02
4550.000	69.14	1.20	20.96	21.83	-147.21	10.02
4600.000	64.52	1.46	14.51	22.10	33.58	9.89
4650.000	67.44	1.37	16.14	22.08	-143.23	9.84
4700.000	77.06	1.36	16.34	22.33	39.37	9.84
4750.000	88.90	1.26	18.34	21.82	-137.43	9.91
4800.000	72.59	1.24	19.40	21.50	42.57	9.96
4850.000	74.27	1.15	23.19	21.17	-135.85	9.93
4900.000	76.08	1.56	13.16	20.66	44.96	10.06
4950.000	70.69	1.73	11.50	19.92	-138.13	10.29
5000.000	71.99	1.40	15.56	19.39	34.51	10.30
5050.000	80.80	1.54	13.45	20.36	-151.67	10.21
5100.000	75.37	1.46	14.50	21.19	27.05	9.90
5150.000	83.45	1.60	12.79	21.70	-148.42	9.87
5200.000	72.77	1.48	14.23	21.64	31.83	9.99
5250.000	69.52	1.49	14.18	21.72	-147.55	9.86
5300.000	74.62	1.51	13.78	21.46	36.21	10.00
5350.000	71.45	1.45	14.67	21.15	-147.61	10.13
5400.000	75.71	1.51	13.96	20.86	31.36	10.14
5450.000	70.91	1.52	13.71	20.81	-152.57	10.17
5500.000	72.63	1.34	16.74	21.28	25.39	10.07
5550.000	73.60	1.43	15.12	21.25	-155.06	10.05
5600.000	82.44	1.03	37.95	20.98	23.42	10.69
5650.000	74.99	1.23	19.69	20.33	-153.33	10.30
5700.000	78.70	1.35	16.47	20.77	12.71	10.32
5750.000	78.09	1.50	13.96	21.59	-169.89	10.12
5800.000	77.81	1.86	10.47	22.29	8.22	9.90
5850.000	72.90	2.15	8.73	22.39	-158.35	9.97
5900.000	63.28	2.01	9.51	22.12	9.40	10.07
5950.000	76.19	2.14	8.82	21.96	-169.05	10.11
6000.000	81.14	1.86	10.86	21.02	5.49	3.70
6250.000	75.83	1.53	13.42	24.13	151.36	2.37
6500.000	77.88	2.12	8.89	25.13	-51.81	2.41
6750.000	75.55	1.16	22.58	28.23	73.09	2.33
7000.000	69.47	1.44	14.95	36.53	-120.19	2.18
7250.000	70.54	1.80	10.39	46.68	45.64	1.92
7500.000	74.79	1.53	13.56	45.56	-116.39	-.02

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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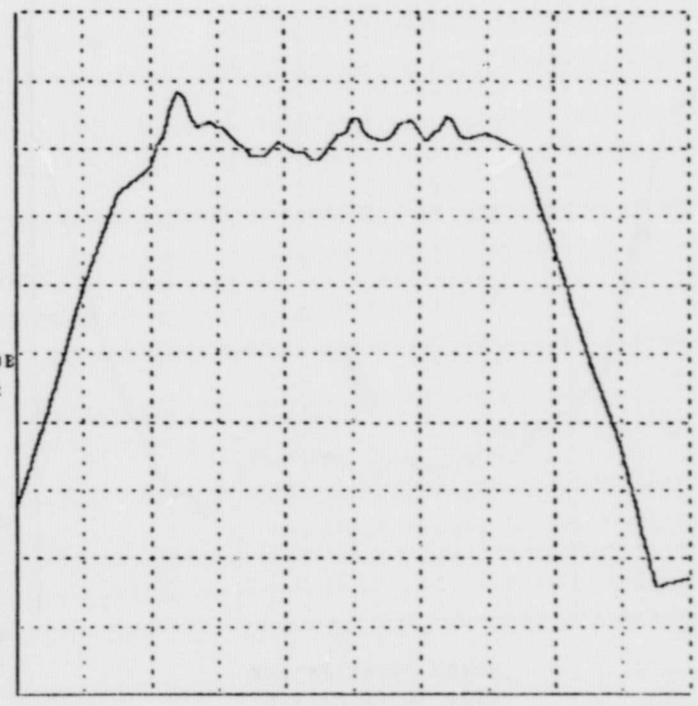
NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#9 IN-17 OUT-3



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#9 IN-17 OUT-3

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	82.28	1.25	19.21	46.24	103.20	.61
2750.000	76.37	1.24	19.35	38.74	41.29	.81
3000.000	82.02	1.37	16.12	30.30	-42.70	1.05
3250.000	87.57	1.10	26.65	23.33	-147.90	1.19
3500.000	80.75	1.34	16.82	21.43	102.97	2.51
3550.000	76.33	1.18	21.72	19.75	-58.77	9.05
3600.000	84.00	1.73	11.49	19.18	137.32	9.10
3650.000	78.04	1.76	11.03	17.06	-26.49	9.54
3700.000	67.26	1.20	20.76	15.64	153.75	9.87
3750.000	78.69	1.34	16.76	16.19	-21.87	9.58
3800.000	75.13	1.04	34.23	17.65	168.72	9.16
3850.000	72.42	1.45	14.67	18.40	8.16	8.97
3900.000	73.10	1.23	19.60	18.12	-154.2?	9.17
3950.000	73.66	1.18	21.57	18.06	37.97	9.23
4000.000	85.15	1.43	15.03	16.42	-126.67	9.18
4050.000	71.11	1.56	13.23	18.55	67.51	9.16
4100.000	76.84	1.35	16.60	19.10	-97.20	9.14
4150.000	69.38	1.69	11.83	19.65	96.45	9.02
4200.000	79.55	1.51	13.61	19.86	-61.95	9.01
4250.000	68.36	1.42	15.25	20.54	134.24	8.92
4300.000	61.04	1.26	18.78	20.52	-23.08	8.89
4350.000	76.44	1.22	20.15	20.48	174.04	6.93
4400.000	90.77	1.20	20.80	20.03	15.26	9.05
4450.000	67.73	1.42	15.19	19.41	-151.72	9.25
4500.000	66.14	1.74	11.34	19.84	42.35	9.13
4550.000	69.96	1.62	12.53	20.17	-120.50	9.02
4600.000	65.17	1.38	15.87	20.29	77.66	9.01
4650.000	67.03	1.11	25.74	20.26	-64.84	9.04
4700.000	73.66	1.25	19.13	20.74	112.24	8.92
4750.000	72.99	1.14	23.75	20.76	-45.78	6.86
4800.000	74.05	1.50	14.02	20.30	153.28	8.93
4850.000	78.40	1.49	14.09	19.57	-7.32	9.10
4900.000	70.15	1.14	23.65	18.92	-174.25	9.21
4950.000	70.42	1.53	13.53	18.87	21.30	9.12
5000.000	67.17	1.61	12.66	17.75	-142.50	9.44
5050.000	72.92	1.48	14.32	17.73	41.50	9.48
5100.000	67.35	1.37	16.10	18.60	-123.86	9.08
5150.000	72.70	1.29	17.99	19.21	74.60	9.04
5200.000	75.94	1.46	14.62	19.30	-89.15	9.05
5250.000	65.25	1.29	17.93	19.29	106.66	8.97
5300.000	79.06	1.34	16.65	18.97	-52.09	9.12
5350.000	78.10	1.12	24.65	18.23	146.55	9.33
5400.000	70.46	1.26	16.69	18.01	-27.80	9.38
5450.000	69.96	1.49	14.10	17.97	163.05	9.38
5500.000	71.31	1.85	10.49	18.74	-5.30	9.19
5550.000	71.72	1.99	9.57	19.40	-167.74	8.90
5600.000	75.19	1.54	13.46	18.05	31.45	9.10
5650.000	72.03	1.16	26.19	13.59	-133.26	9.32
5700.000	71.14	1.12	25.15	17.66	33.92	9.54
5750.000	73.57	1.69	11.63	17.97	-118.78	9.52
5800.000	79.22	2.42	7.65	19.00	73.23	9.16
5850.000	76.64	2.39	7.73	19.27	-68.63	9.14
5900.000	74.04	2.45	7.53	19.13	134.16	9.30
5950.000	80.65	2.13	8.87	18.95	-63.56	9.38
6000.000	75.61	1.72	11.52	18.98	126.43	2.82
6250.000	75.16	1.53	13.61	19.95	-3.43	1.39
6500.000	81.59	1.04	10.55	27.21	-159.96	1.41
6750.000	71.03	1.19	21.07	34.58	97.21	1.37
7000.000	71.86	1.66	12.12	42.19	7.37	1.14
7250.000	74.83	3.23	5.56	52.05	-106.29	1.04
7500.000	79.17	1.19	21.07	51.41	-179.76	1.04

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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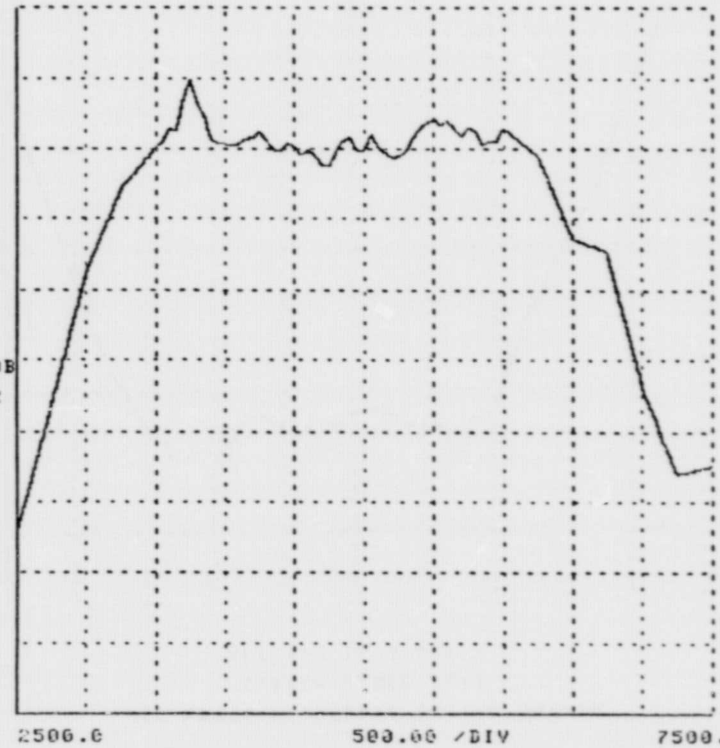
NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#11 IN-21 OUT-3



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#11 IN-21 OUT-3

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	93.77	1.26	18.84	47.17	64.66	.21
2750.000	83.98	1.18	21.79	36.36	50.36	.21
3000.000	93.91	1.19	21.11	26.95	26.17	.39
3250.000	85.13	1.09	27.12	22.82	-20.12	.57
3500.000	70.88	1.23	19.69	19.98	-75.67	1.06
3550.000	80.31	1.18	21.86	19.48	136.82	0.40
3600.000	73.0[illegible]	1.33	16.88	18.60	-16.40	0.41
3650.000	79.77	1.93	9.95	18.75	-165.99	0.32
3700.000	70.09	1.46	14.52	16.41	42.00	0.09
3750.000	79.97	1.28	18.27	15.13	-126.09	9.19
3800.000	72.08	1.26	18.66	16.78	71.30	0.82
3850.000	68.62	1.37	16.19	17.74	-83.57	0.44
3900.000	63.49	1.59	12.85	19.37	127.44	0.20
3950.000	74.27	1.50	13.98	19.59	-18.71	0.16
4000.000	75.55	1.45	14.60	19.60	-166.96	6.26
4050.000	73.47	1.56	12.96	19.78	43.98	0.24
4100.000	73.33	1.33	16.89	19.63	-103.47	0.34
4150.000	71.32	1.71	11.66	19.34	103.89	0.33
4200.000	73.92	1.71	11.62	19.25	-43.32	0.42
4250.000	65.72	1.22	20.12	18.76	160.79	0.58
4300.000	63.16	1.12	24.86	19.45	7.93	0.39
4350.000	73.63	1.20	21.02	20.07	-140.77	6.20
4400.000	85.21	1.44	14.82	20.09	72.60	0.24
4450.000	66.42	1.27	16.44	19.62	-77.36	0.43
4500.000	75.25	1.02	35.01	19.85	129.17	0.41
4550.000	73.75	1.25	18.97	20.42	-20.14	0.26
4600.000	67.64	1.16	22.70	20.18	-168.25	0.35
4650.000	67.68	1.26	16.74	20.46	39.23	0.32
4700.000	70.21	1.16	22.42	21.20	-107.64	0.05
4750.000	70.71	1.18	21.78	21.14	109.51	0.09
4800.000	72.09	1.27	18.37	20.14	-39.04	0.34
4850.000	63.71	1.25	19.14	19.46	169.23	0.53
4900.000	71.13	1.10	26.21	19.26	13.74	0.58
4950.000	73.73	1.33	16.92	20.09	-139.75	6.24
5000.000	70.11	1.82	10.72	20.06	77.19	0.27
5050.000	83.16	1.61	12.58	18.98	-77.39	6.62
5100.000	71.03	1.71	11.67	19.83	126.68	6.44
5150.000	76.47	1.35	16.51	20.30	-21.40	0.24
5200.000	76.26	1.64	12.27	20.62	-170.05	6.16
5250.000	71.07	1.60	12.75	20.58	44.23	0.15
5300.000	79.84	1.22	20.21	20.15	-103.37	0.24
5350.000	77.94	1.13	24.29	19.24	107.56	6.44
5400.000	74.14	1.10	26.10	18.54	-47.10	0.56
5450.000	70.19	1.35	16.50	18.23	159.26	0.56
5500.000	70.66	1.69	11.35	17.79	3.99	0.66
5550.000	70.66	2.05	9.25	18.26	-132.67	3.56
5600.000	69.74	1.73	11.46	13.04	33.71	3.57
5650.000	72.06	1.30	17.31	13.61	-191.12	3.54
5700.000	68.32	1.43	15.03	15.07	198.31	6.34
5750.000	60.15	1.52	13.72	18.52	-41.32	3.62
5800.000	67.25	1.57	13.12	18.72	157.87	3.63
5850.000	69.27	2.00	9.53	19.68	9.16	3.34
5900.000	64.70	1.79	10.95	19.51	-142.23	3.33
5950.000	69.42	1.74	11.39	19.49	67.59	3.46
6000.000	68.04	1.66	12.13	18.55	-57.31	2.30
6250.000	73.64	1.71	11.63	20.32	-147.96	.78
6500.000	76.04	2.16	8.71	26.39	132.61	.60
6750.000	68.81	1.54	13.40	27.32	163.90	.44
7000.000	71.99	1.35	16.62	36.94	52.61	.44
7250.000	71.70	2.08	9.10	42.99	24.65	.32
7500.000	73.39	1.15	23.29	42.43	-4.94	.32

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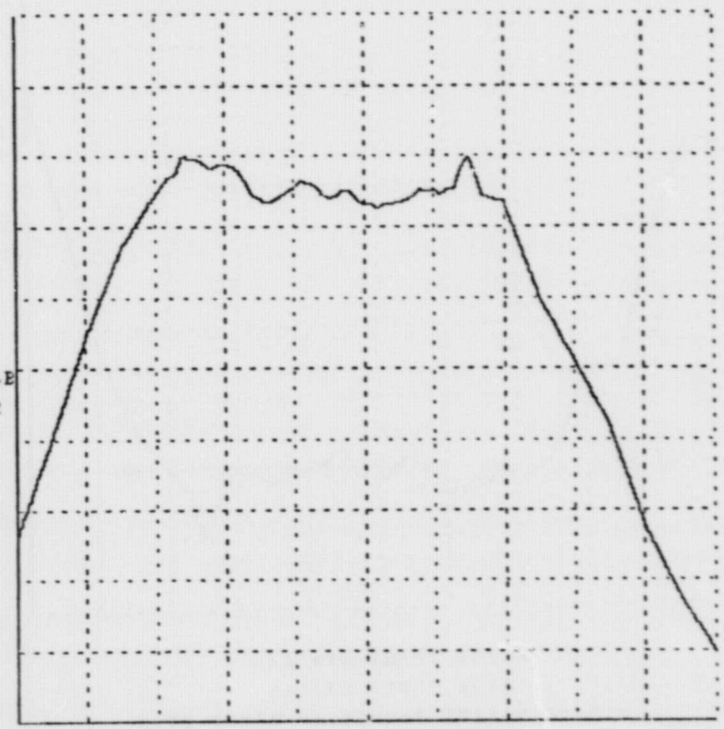

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#13 IN-3 OUT-4

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	95.30	1.32	17.14	46.92	-39.37	.95
2750.000	84.21	1.65	31.93	40.12	64.76	2.95
3000.000	84.86	1.42	15.29	32.93	149.79	3.16
3250.000	89.54	1.10	26.24	26.57	-143.54	3.31
3500.000	80.63	1.16	26.14	22.79	-86.53	4.70
3550.000	79.35	1.39	15.71	22.19	68.96	11.43
3600.000	78.57	1.51	13.82	21.55	-138.02	11.36
3650.000	76.35	1.70	11.66	21.32	20.08	11.40
3700.000	76.39	1.24	19.35	20.12	171.56	11.60
3750.000	75.63	1.48	14.22	20.26	-37.55	11.52
3800.000	76.04	1.23	19.77	20.22	116.87	11.47
3850.000	74.30	1.44	14.91	20.59	-90.51	11.36
3900.000	74.26	1.45	14.68	20.93	67.28	11.28
3950.000	70.76	1.36	15.94	20.69	-136.50	11.36
4000.000	74.96	1.51	13.79	20.67	16.39	11.40
4050.000	72.01	1.45	14.77	20.72	173.24	11.44
4100.000	72.84	1.15	23.03	21.05	-33.48	11.45
4150.000	71.99	1.57	13.12	21.67	120.87	11.24
4200.000	79.61	1.32	17.11	22.74	-76.20	11.10
4250.000	70.97	1.13	24.05	22.95	81.37	11.11
4300.000	72.95	1.44	14.88	23.26	-118.25	11.07
4350.000	70.47	1.47	14.37	23.14	42.87	11.11
4400.000	66.37	1.32	17.16	22.91	-156.28	11.17
4450.000	70.77	1.04	34.61	22.47	.56	11.27
4500.000	67.09	1.25	19.00	22.23	155.53	11.35
4550.000	66.05	1.29	17.91	21.69	-47.86	11.40
4600.000	65.27	1.49	14.13	21.96	105.57	11.45
4650.000	67.01	1.49	14.07	22.02	-100.09	11.33
4700.000	75.25	1.36	16.41	22.71	57.57	11.20
4750.000	72.49	1.25	19.13	22.55	-143.32	11.16
4800.000	65.03	1.29	18.04	22.87	15.63	11.25
4850.000	77.52	1.26	18.80	22.43	171.83	11.36
4900.000	61.48	1.19	21.19	22.53	-33.42	11.43
4950.000	78.96	1.32	17.19	23.02	120.31	11.27
5000.000	79.34	1.44	14.80	23.41	-79.06	11.22
5050.000	65.10	1.32	17.14	23.33	76.51	11.24
5100.000	74.93	1.61	12.63	23.64	-123.64	11.22
5150.000	77.65	1.18	21.79	23.33	32.66	11.32
5200.000	77.53	1.47	14.36	23.33	-171.19	11.26
5250.000	81.29	1.52	13.73	23.30	-13.28	11.29
5300.000	80.03	1.24	19.42	23.11	142.53	11.30
5350.000	82.94	1.30	17.68	22.90	-60.20	11.37
5400.000	78.84	1.05	32.42	22.40	93.16	11.50
5450.000	76.44	1.21	20.38	22.50	-114.07	11.46
5500.000	75.73	1.36	16.39	22.40	40.77	11.42
5550.000	80.77	1.66	12.12	22.67	-165.11	11.40
5600.000	85.36	1.44	14.80	22.35	-9.76	11.35
5650.000	78.36	1.37	16.09	22.23	145.44	11.46
5700.000	74.91	1.43	14.33	20.75	-62.36	11.79
5750.000	80.87	1.40	15.63	20.14	81.96	12.11
5800.000	79.13	1.73	11.31	21.25	-135.30	11.79
5850.000	81.36	2.23	3.19	22.31	17.47	11.46
5900.000	77.14	1.89	10.23	22.94	169.64	11.51
5950.000	79.92	2.19	8.55	23.16	-37.01	11.63
6000.000	80.23	1.91	10.03	23.13	110.30	5.07
6250.000	74.79	1.59	12.83	30.00	135.03	3.53
6500.000	69.59	2.11	8.94	34.44	-165.21	3.43
6750.000	74.21	1.37	16.21	38.39	-123.23	3.45
7000.000	74.69	1.31	17.42	45.16	-65.95	3.43
7250.000	77.34	2.91	4.22	51.09	-21.26	3.55
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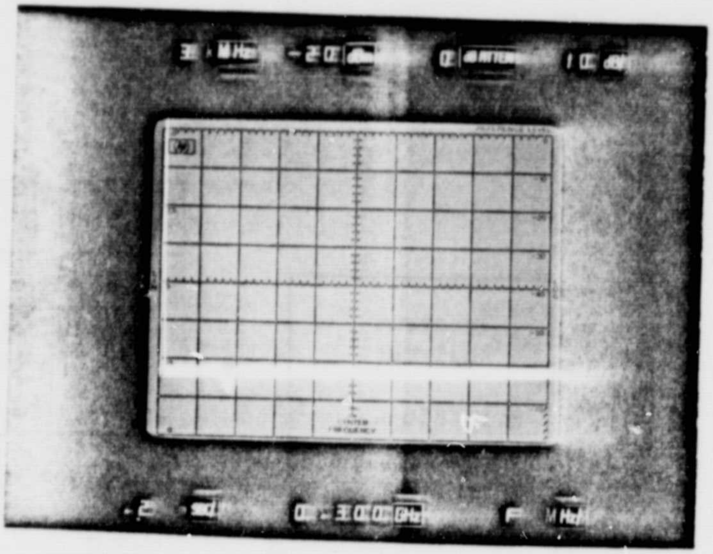
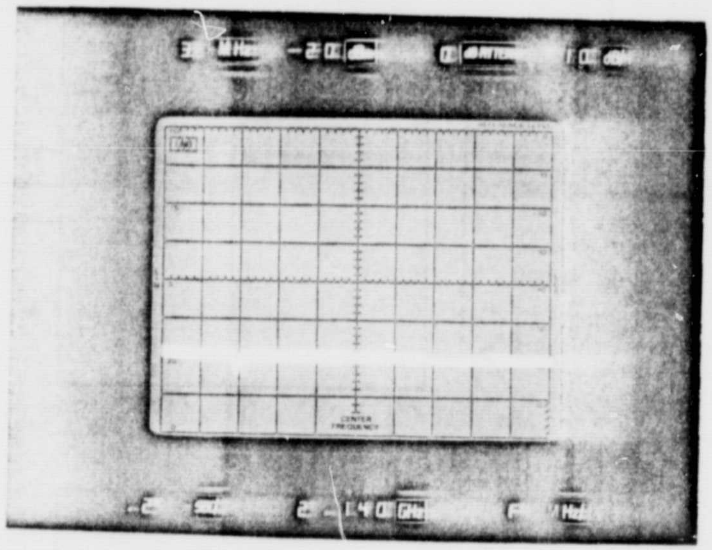
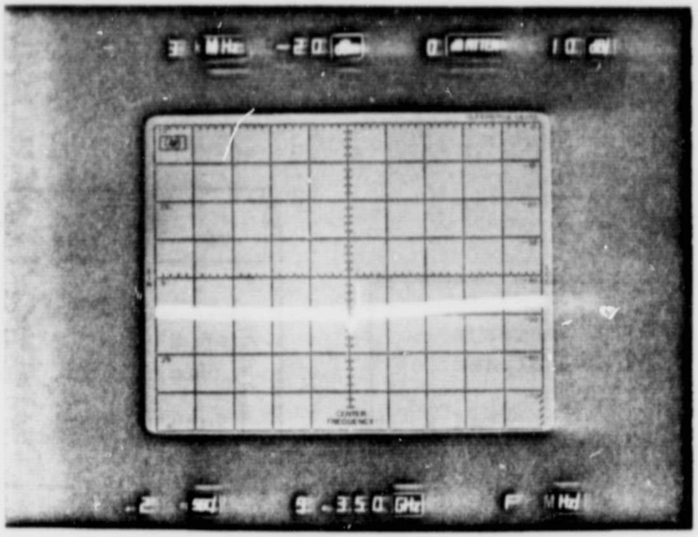


0.01 GHz to 1.8 GHz

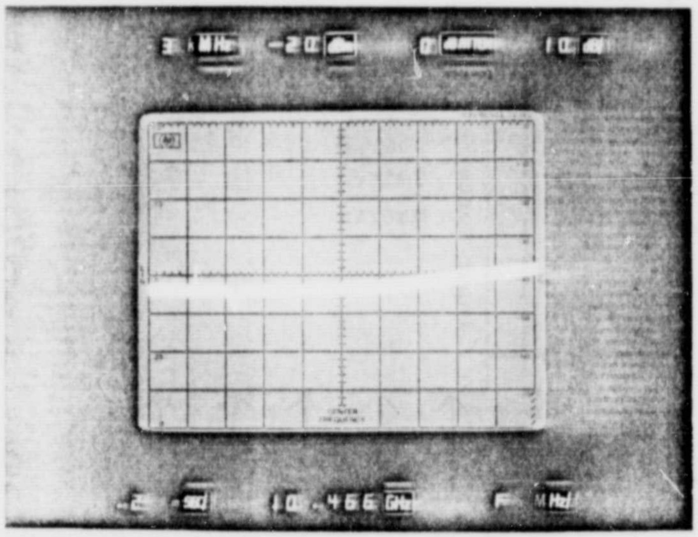


1.7 GHz to 4.1 GHz



Note Second
Harmonic at
9.5 GHz

5.8 GHz to 12.9 GHz



Note Second
Harmonic at
9.5 GHz

8.5 GHz to 18.0 GHz

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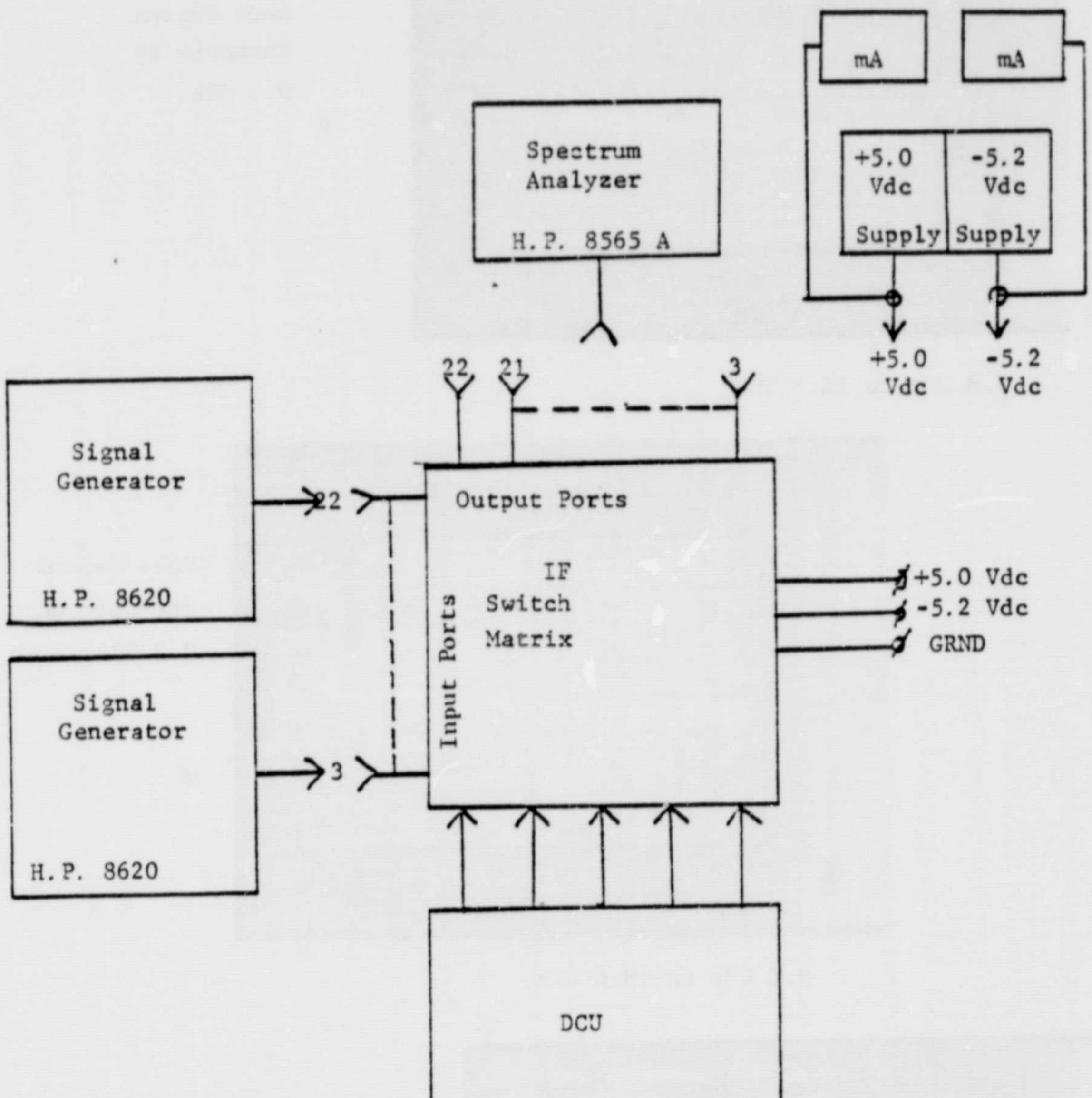

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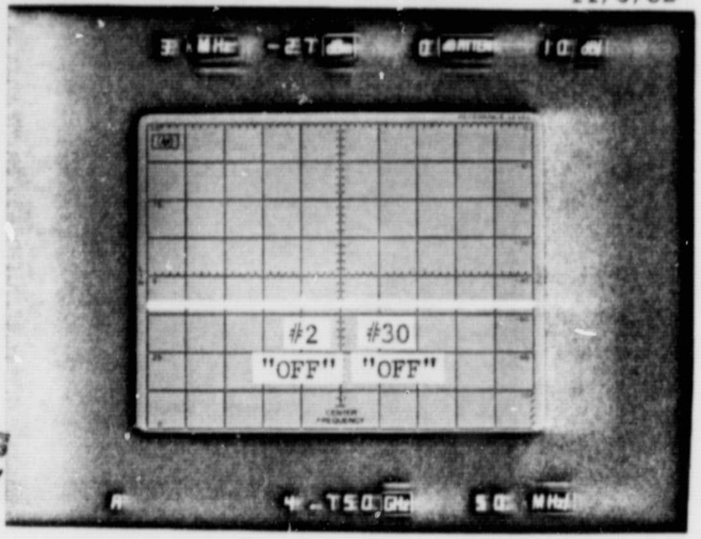

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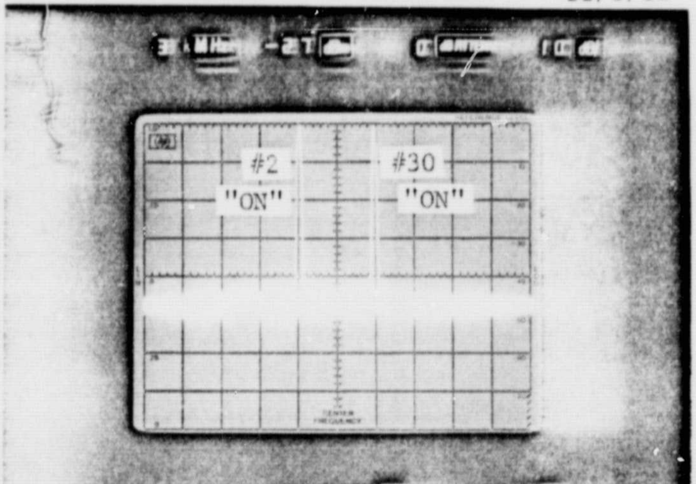

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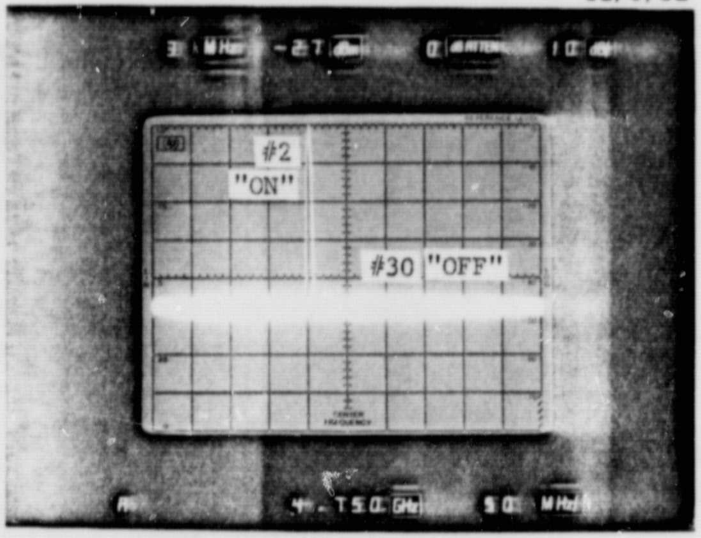

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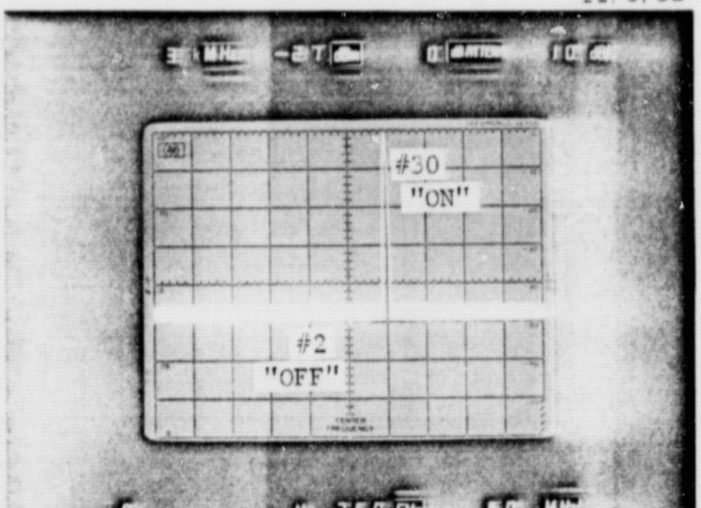

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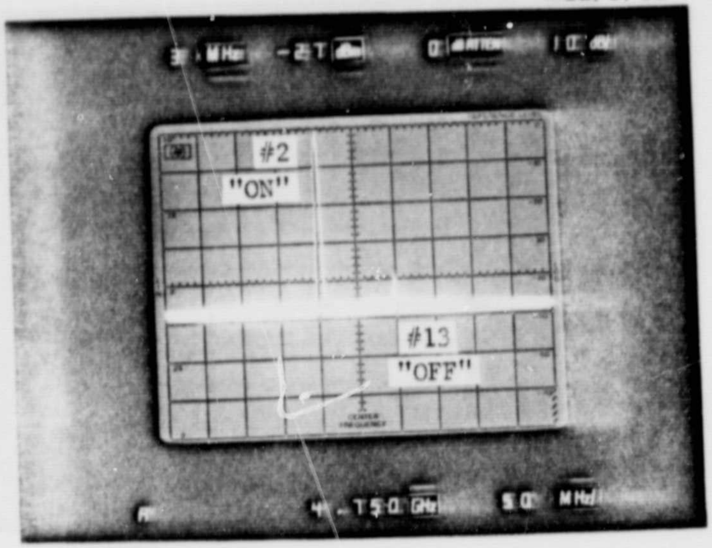

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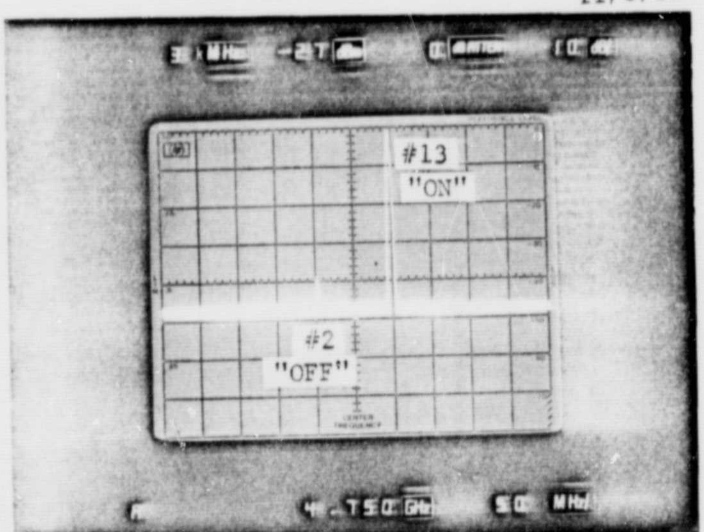
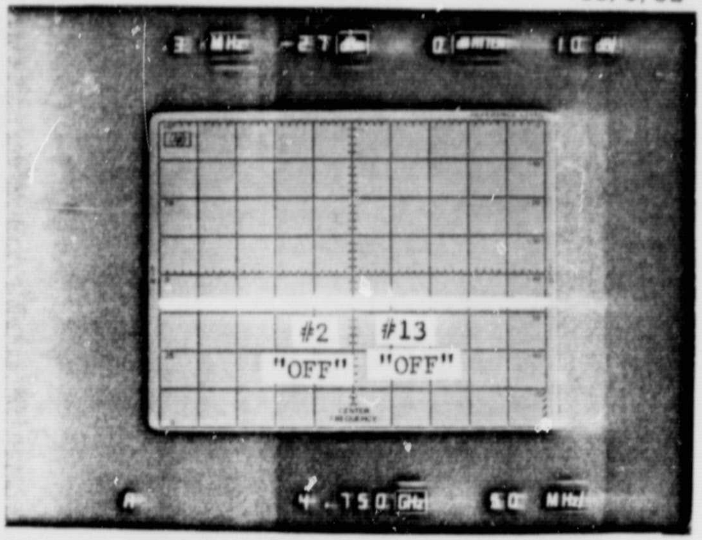


11/6/82



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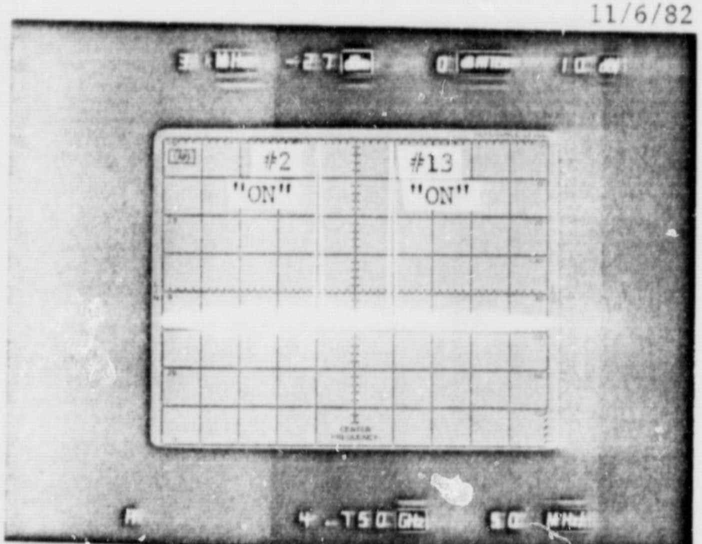
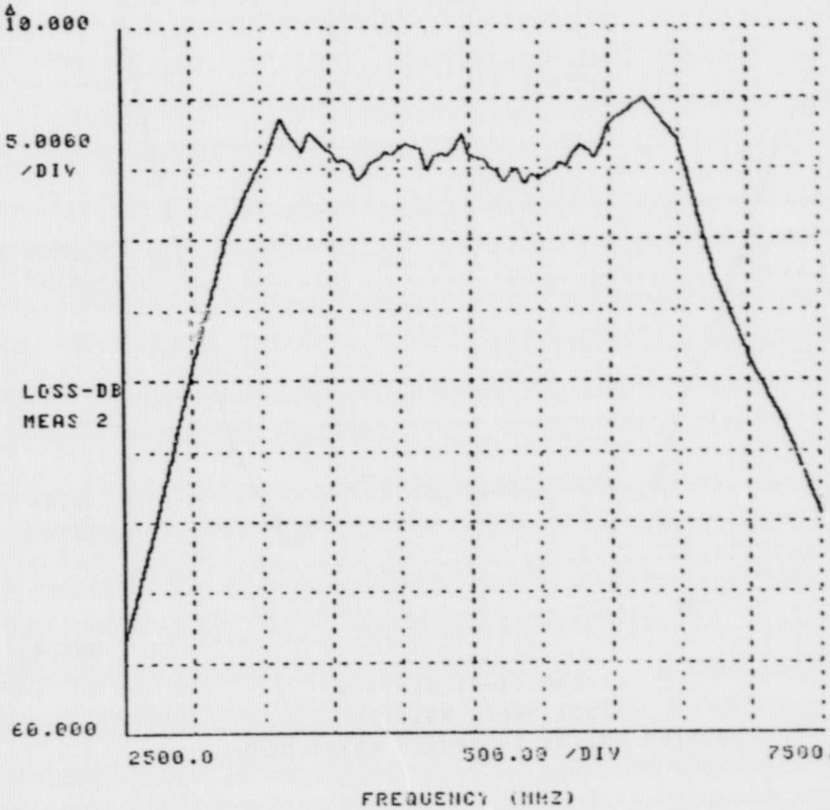


NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#43 IN-7 OUT-13



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#43 IN-7 OUT-13

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	85.92	1.12	24.66	53.65	90.89	1.54
2750.000	94.36	1.53	13.55	44.52	-37.92	1.54
3000.000	87.06	1.12	25.22	34.29	172.98	1.83
3250.000	92.63	1.12	25.08	24.78	-8.13	2.13
3500.000	78.68	1.23	19.82	19.60	150.19	2.87
3550.000	81.38	1.13	24.57	19.08	41.78	5.96
3600.000	80.35	1.30	17.77	17.66	-64.60	6.38
3650.000	62.46	1.41	15.31	16.36	172.13	6.59
3700.000	74.25	1.43	15.03	17.46	56.12	6.25
3750.000	84.96	1.11	26.01	18.11	-53.01	5.86
3800.000	79.06	1.31	17.55	18.79	-152.95	5.98
3850.000	79.55	1.48	14.32	17.44	98.33	6.21
3900.000	76.21	1.35	16.51	17.67	-16.47	6.16
3950.000	75.46	1.29	16.07	18.38	-123.59	6.02
4000.000	69.76	1.28	16.13	16.71	126.93	5.94
4050.000	74.06	1.13	24.25	19.44	22.56	5.74
4100.000	73.69	1.22	20.12	19.40	-79.63	5.90
4150.000	73.82	1.12	25.14	19.65	170.23	5.65
4200.000	75.07	1.26	18.34	20.85	69.39	5.54
4250.000	76.64	1.29	18.05	20.34	-29.14	5.63
4300.000	67.77	1.12	24.75	19.52	-133.16	5.62
4350.000	73.89	1.11	25.36	19.33	121.23	5.53
4400.000	81.18	1.16	22.86	18.63	13.33	5.96
4450.000	81.71	1.23	19.71	16.91	-93.30	5.87
4500.000	69.41	1.27	16.30	16.51	161.87	5.99
4550.000	65.55	1.15	23.21	16.20	51.22	6.03
4600.000	66.17	1.12	25.22	18.47	-55.11	6.02
4650.000	69.81	1.22	19.96	18.58	-165.60	5.69
4700.000	66.18	1.10	26.75	20.08	92.97	5.60
4750.000	70.85	1.33	17.01	19.10	-7.06	5.83
4800.000	76.56	1.14	23.67	18.96	-116.98	5.67
4850.000	61.31	1.06	30.17	19.04	141.60	5.76
4900.000	64.11	1.11	25.66	18.47	35.50	5.95
4950.000	59.30	1.33	16.93	17.52	-72.62	6.19
5000.000	77.23	1.15	23.02	19.06	172.76	5.96
5050.000	77.64	1.22	19.92	19.22	72.74	5.88
5100.000	74.64	1.14	23.49	19.33	-38.90	5.96
5150.000	66.99	1.16	22.44	19.94	-141.66	5.79
5200.000	71.43	1.28	18.12	20.13	112.78	5.77
5250.000	79.36	1.16	22.78	20.93	10.63	5.57
5300.000	73.66	1.17	22.21	20.19	-67.91	5.50
5350.000	69.48	1.36	16.39	20.05	158.31	5.91
5400.000	73.09	1.26	19.33	21.09	59.29	5.66
5450.000	68.87	1.43	14.98	20.35	-45.33	5.63
5500.000	68.70	1.34	16.65	20.74	-150.50	5.72
5550.000	73.03	1.32	17.25	20.36	196.70	5.74
5600.000	72.05	1.10	26.74	20.06	2.71	5.39
5650.000	75.44	1.32	17.15	19.55	-105.31	5.94
5700.000	83.76	1.11	26.03	19.64	149.03	3.78
5750.000	86.29	1.13	24.45	18.79	46.70	3.97
5800.000	73.68	1.31	17.46	13.32	-65.93	6.21
5850.000	76.70	1.70	11.66	13.67	-176.73	5.95
5900.000	75.75	1.74	11.36	13.24	79.75	3.64
5950.000	76.24	1.93	9.98	18.38	-19.94	5.97
6000.000	79.36	1.63	12.39	16.83	-135.29	2.32
6250.000	67.23	1.04	33.92	15.00	35.31	2.31
6500.000	79.04	1.20	20.73	15.01	169.13	2.23
6750.000	77.78	1.24	19.47	27.27	-5.30	2.93
7000.000	75.55	1.50	12.94	33.50	163.97	2.05
7250.000	71.45	1.14	23.45	38.01	-13.56	1.94
7500.000	77.09	1.30	17.68	44.37	173.95	-.06

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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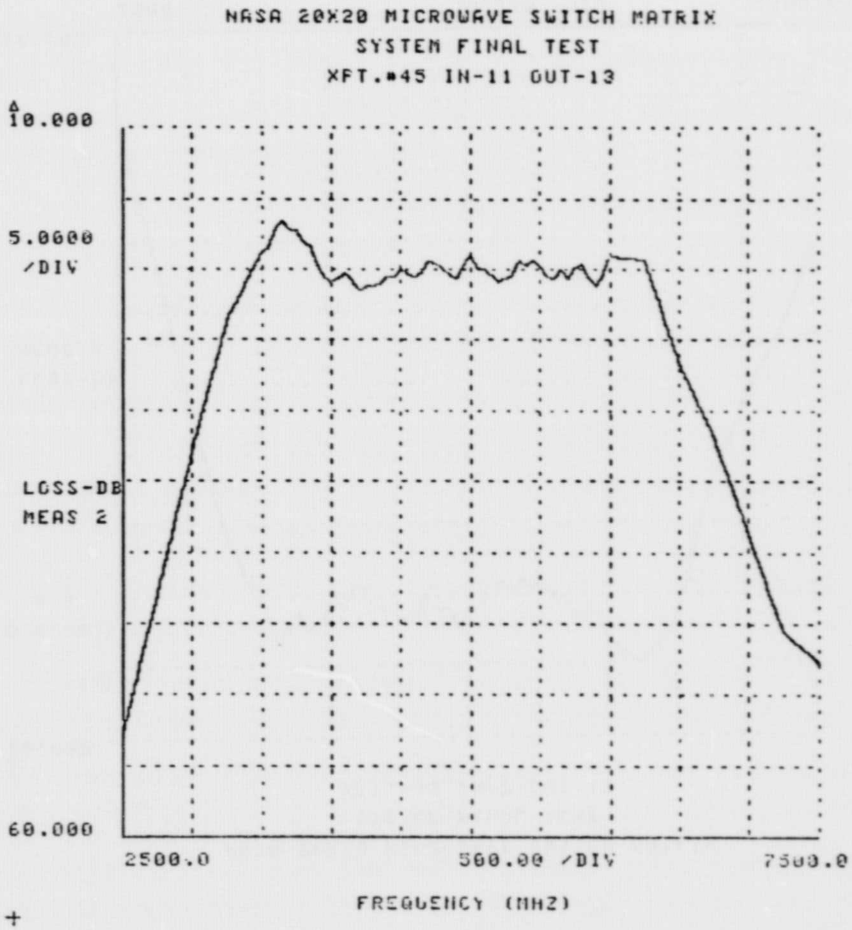

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OF POOR QUALITY

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#45 IN-11 OUT-13

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	82.81	1.13	24.44	52.64	-7.43	.91
2750.000	69.44	1.02	40.13	42.98	-83.07	.91
3000.000	81.39	1.35	16.50	33.08	-171.91	1.20
3250.000	88.02	1.16	22.41	23.52	60.39	1.50
3500.000	75.19	1.27	18.50	18.80	-81.67	2.20
3550.000	74.63	1.29	18.65	18.49	-177.56	5.38
3600.000	73.22	1.15	23.29	17.03	84.65	5.74
3650.000	86.10	1.58	13.00	16.61	-24.10	5.62
3700.000	74.72	1.60	12.68	17.25	-124.96	5.54
3750.000	91.46	1.22	20.26	17.32	136.55	5.48
3800.000	62.22	1.15	23.30	18.06	37.72	5.51
3850.000	84.60	1.21	26.54	18.37	-61.77	5.44
3900.000	76.89	1.26	18.81	19.71	-158.28	5.19
3950.000	78.92	1.09	27.42	20.57	111.58	4.99
4000.000	73.57	1.11	25.63	20.65	21.95	5.03
4050.000	65.72	1.09	27.04	20.62	-69.37	5.15
4100.000	76.21	1.24	19.55	20.32	-163.62	5.27
4150.000	72.03	1.06	30.19	20.84	100.77	5.14
4200.000	72.92	1.36	16.02	21.46	11.45	5.01
4250.000	74.57	1.27	18.51	21.21	-79.66	5.06
4300.000	73.06	1.16	22.49	21.14	-170.62	5.03
4350.000	78.45	1.07	29.75	20.97	95.37	5.14
4400.000	62.07	1.46	15.51	20.51	4.47	5.21
4450.000	66.62	1.52	13.75	20.56	-88.19	5.16
4500.000	66.29	1.24	19.25	19.97	178.71	5.26
4550.000	68.89	1.21	20.27	20.33	82.59	5.15
4600.000	69.96	1.50	13.96	20.55	-6.83	5.10
4650.000	75.42	1.42	15.20	20.23	-101.01	5.16
4700.000	66.49	1.40	15.55	19.44	167.43	5.32
4750.000	73.31	1.27	16.48	19.37	67.55	5.37
4800.000	76.24	1.25	19.69	19.93	-25.93	5.15
4850.000	68.39	1.13	24.30	20.37	-117.99	5.15
4900.000	64.81	1.57	13.10	20.60	148.77	4.96
4950.000	67.29	1.74	11.35	19.65	63.59	5.19
5000.000	72.08	1.40	15.65	16.96	-37.91	5.50
5050.000	69.19	1.53	13.63	19.89	-134.40	5.27
5100.000	68.65	1.47	14.47	19.95	132.32	5.18
5150.000	69.86	1.59	12.64	20.40	39.05	5.13
5200.000	70.45	1.48	14.31	20.67	-52.47	5.03
5250.000	67.04	1.46	14.56	20.59	-142.07	5.01
5300.000	68.71	1.54	13.46	20.42	127.06	5.18
5350.000	82.26	1.42	15.20	19.37	31.34	5.38
5400.000	75.51	1.50	13.99	19.72	-66.53	5.32
5450.000	72.48	1.55	13.27	19.40	-160.31	5.38
5500.000	81.49	1.31	17.48	19.76	99.79	5.34
5550.000	81.50	1.41	15.42	20.50	7.58	5.09
5600.000	72.73	1.05	31.81	20.65	-93.23	5.14
5650.000	69.03	1.24	19.47	19.99	-177.34	5.27
5700.000	76.65	1.33	17.00	20.64	87.08	5.17
5750.000	69.60	1.54	13.31	19.92	-3.57	5.33
5800.000	73.40	1.82	10.74	19.63	-194.77	5.50
5850.000	70.24	2.17	8.67	20.61	152.38	5.17
5900.000	72.63	1.96	9.80	21.16	69.08	4.92
5950.000	81.47	2.15	8.77	20.41	-18.67	5.19
6000.000	70.60	1.83	10.64	19.11	-117.34	2.44
6250.000	71.04	1.51	13.88	19.29	73.29	1.53
6500.000	90.07	2.12	8.89	26.60	-32.75	1.41
6750.000	80.68	1.13	24.05	31.73	-174.83	1.25
7000.000	69.67	1.41	15.39	38.94	99.80	1.06
7250.000	76.92	1.32	10.72	43.57	-6.49	1.13
7500.000	77.49	1.53	13.52	47.76	-104.25	1.13

REF PLANE EXT(CM): INPUT= .00 TRAN= .09

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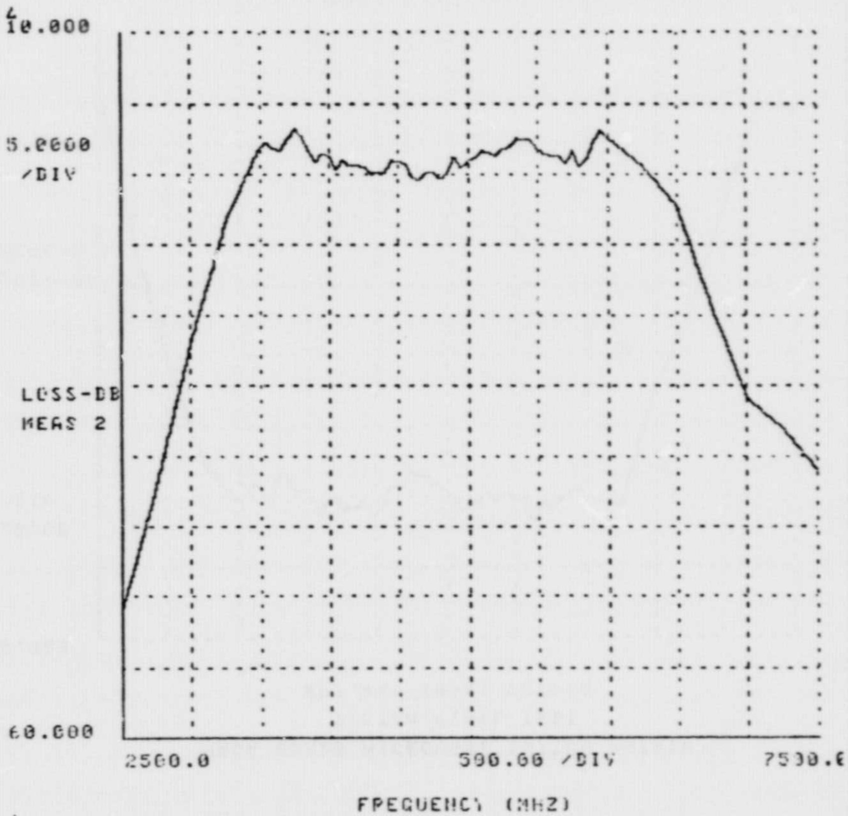
NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#47 IN-17 OUT-13

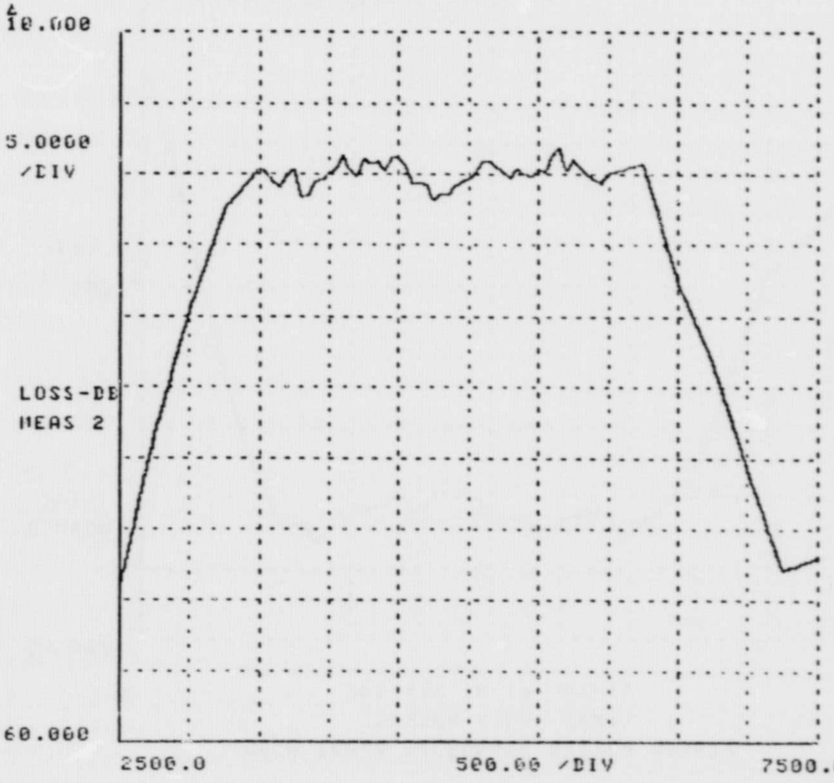


NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#47 IN-17 OUT-13

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	80.94	1.20	20.68	51.10	46.67	.04
2750.000	90.93	1.17	22.32	42.31	51.49	.04
3000.000	64.23	1.34	16.76	32.29	40.31	.28
3250.000	65.29	1.13	24.52	23.43	1.77	.59
3500.000	80.82	1.29	17.93	16.05	-66.20	1.41
3550.000	77.02	1.21	20.27	17.75	-150.11	4.61
3600.000	75.85	1.58	12.95	18.20	127.63	4.46
3650.000	99.38	1.63	10.67	18.30	49.23	4.36
3700.000	74.61	1.26	18.84	17.51	-29.01	4.62
3750.000	76.23	1.36	16.41	16.76	-116.94	4.73
3800.000	75.94	1.06	27.96	17.29	160.78	4.62
3850.000	74.56	1.41	15.32	18.26	76.77	4.36
3900.000	75.67	1.26	18.16	19.12	3.75	4.19
3950.000	74.66	1.19	21.04	16.55	-73.94	4.44
4000.000	72.57	1.42	15.28	18.66	-156.01	4.36
4050.000	77.71	1.53	13.52	19.72	129.24	4.16
4100.000	69.04	1.38	15.94	16.94	54.23	4.35
4150.000	102.47	1.64	12.33	19.40	-27.32	4.29
4200.000	75.29	1.62	12.53	19.41	-100.31	4.26
4250.000	82.17	1.37	16.04	19.41	179.41	4.31
4300.000	70.37	1.25	19.20	19.98	104.40	4.16
4350.000	73.29	1.18	21.59	19.80	28.99	4.17
4400.000	65.03	1.20	20.86	19.87	-45.60	4.19
4450.000	78.16	1.42	15.24	18.97	-121.92	4.34
4500.000	67.60	1.77	11.15	19.14	158.13	4.48
4550.000	70.13	1.61	12.61	19.21	76.97	4.37
4600.000	70.60	1.32	17.21	20.16	.78	4.11
4650.000	68.11	1.12	24.86	20.39	-70.95	4.08
4700.000	72.49	1.22	19.97	19.86	-146.27	4.27
4750.000	67.33	1.28	20.83	19.88	135.27	4.23
4800.000	85.60	1.47	14.43	20.26	61.60	4.01
4850.000	56.69	1.46	14.20	19.97	-6.90	4.19
4900.000	60.48	1.13	24.34	16.80	-69.16	4.47
4950.000	63.83	1.52	13.76	19.46	-169.95	4.27
5000.000	61.83	1.71	11.66	19.00	117.27	4.16
5050.000	63.36	1.37	16.07	18.77	39.75	4.29
5100.000	63.72	1.45	14.66	18.34	-37.09	4.42
5150.000	66.82	1.25	19.19	18.46	-119.45	4.30
5200.000	62.04	1.45	14.70	18.60	167.97	4.22
5250.000	81.63	1.34	16.72	18.14	88.81	4.32
5300.000	72.12	1.30	17.67	16.07	12.46	4.35
5350.000	71.47	1.11	26.04	17.44	-67.74	4.50
5400.000	73.86	1.25	19.03	17.54	-149.47	4.46
5450.000	68.80	1.55	13.27	17.55	131.60	4.47
5500.000	72.26	1.60	10.85	18.21	49.70	4.40
5550.000	75.89	1.95	9.96	18.51	-26.65	4.26
5600.000	71.59	1.57	13.10	18.69	-103.31	4.28
5650.000	69.91	1.09	28.19	18.73	179.30	4.23
5700.000	71.80	1.12	24.98	19.22	103.57	4.23
5750.000	70.59	1.64	12.32	19.35	25.22	4.39
5800.000	75.15	2.47	7.46	19.41	-54.39	4.16
5850.000	68.73	2.47	7.47	18.97	-124.36	4.05
5900.000	77.89	2.25	8.32	17.76	153.68	4.57
5950.000	61.38	2.21	9.46	16.89	70.82	4.83
6000.000	59.91	1.71	11.62	17.36	-15.06	1.26
6250.000	60.17	1.51	13.79	19.45	-65.29	.56
6500.000	62.88	1.06	10.45	22.23	-116.03	.50
6750.000	59.29	1.23	19.67	29.33	-156.03	.27
7000.000	70.24	1.64	12.35	35.91	-154.83	.20
7250.000	71.91	3.26	5.50	37.96	163.02	.29
7500.000	71.00	1.24	19.39	41.07	142.82	.29

REF PLANE EXT(CM): INPUT= .00 TRAN= .39

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#49 IN-21 OUT-13

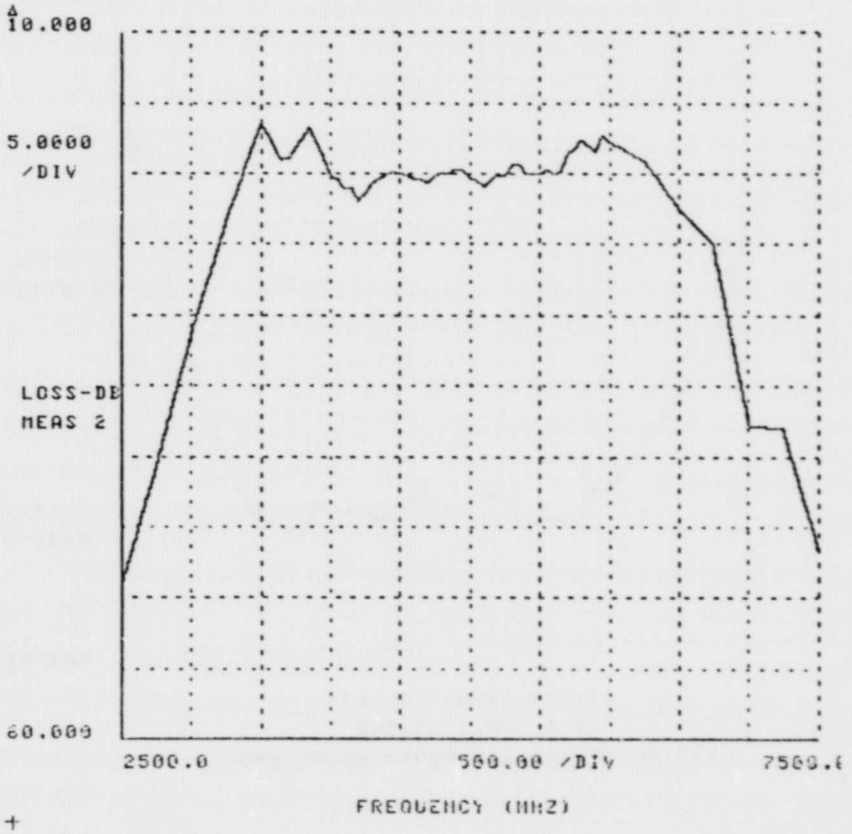


NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#49 IN-21 OUT-13

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	[illegible]5.03	1.27	16.56	49.14	-55.46	1.44
2750.000	77.63	1.13	24.27	38.51	5.75	3.44
3000.000	79.42	1.21	20.63	29.73	44.64	3.73
3250.000	82.48	1.07	29.81	22.41	57.60	1.93
3500.000	79.24	1.24	19.32	19.63	57.59	.65
3550.000	75.28	1.17	22.29	19.86	-12.55	3.86
3600.000	72.99	1.38	15.95	20.57	-81.23	3.62
3650.000	71.61	1.93	10.00	20.87	-142.79	3.52
3700.000	70.42	1.42	15.14	20.06	151.93	3.92
3750.000	75.91	1.33	16.97	19.72	76.05	3.86
3800.000	77.36	1.22	20.16	21.63	12.89	3.36
3850.000	69.36	1.40	15.55	21.50	-42.60	3.34
3900.000	72.70	1.56	13.23	20.51	-107.23	3.68
3950.000	70.61	1.45	14.77	20.40	-175.21	3.64
4000.000	71.11	1.47	14.43	19.96	121.72	3.57
4050.000	70.57	1.63	12.37	19.66	56.43	3.73
4100.000	75.37	1.31	17.36	18.65	-12.55	3.91
4150.000	71.07	1.76	11.17	19.79	-64.27	3.53
4200.000	70.43	1.69	11.80	20.16	-139.64	3.41
4250.000	67.41	1.27	18.45	18.95	152.84	3.77
4300.000	64.49	1.08	28.65	19.26	84.52	3.73
4350.000	70.93	1.21	20.50	19.14	18.44	3.60
4400.000	68.63	1.50	13.94	1[illegible].75	-45.06	3.55
4450.000	65.90	1.25	19.23	18.[illegible]	-105.26	3.73
4500.000	69.97	1.02	39.22	18.86	-179.23	3.90
4550.000	68.09	1.24	19.36	19.40	110.22	3.72
4600.000	67.06	1.17	21.92	20.68	46.82	3.36
4650.000	65.96	1.30	17.79	20.71	-11.53	3.54
4700.000	64.09	1.15	23.31	20.75	-80.56	3.55
4750.000	62.35	1.20	20.82	21.86	-139.45	3.25
4800.000	66.59	1.26	18.66	21.41	162.55	3.34
4850.000	62.74	1.27	18.51	21.48	100.27	3.49
4900.000	58.56	1.09	27.39	20.80	36.78	3.55
4950.000	67.52	1.35	16.48	20.53	-27.42	3.53
5000.000	74.90	1.81	10.80	20.29	-90.42	3.43
5050.000	59.66	1.61	12.64	19.81	-150.66	3.57
5100.000	65.09	1.72	11.57	19.06	141.09	3.90
5150.000	73.85	1.34	16.82	19.07	68.60	3.78
5200.000	63.64	1.67	12.03	19.52	5.10	3.62
5250.000	68.91	1.57	13.11	19.83	-61.85	3.56
5300.000	70.10	1.24	19.47	20.21	-122.80	3.47
5350.000	63.77	1.10	26.41	19.55	173.14	3.69
5400.000	74.06	1.10	26.68	20.01	104.20	3.56
5450.000	63.63	1.36	16.36	20.09	45.11	3.50
5500.000	67.08	1.67	12.02	19.56	-21.94	3.58
5550.000	68.72	2.07	9.13	19.23	-93.59	3.53
5600.000	67.12	1.69	11.36	18.57	-149.12	3.87
5650.000	64.84	1.30	17.73	18.16	137.86	3.98
5700.000	68.65	1.40	15.53	15.76	67.73	3.62
5750.000	65.89	1.50	13.99	18.96	5.88	3.69
5800.000	63.07	1.58	12.92	19.59	-63.29	3.79
5850.000	66.11	1.95	9.82	20.05	-129.65	3.33
5900.000	70.92	1.73	11.05	20.37	157.75	3.30
5950.000	71.02	1.73	11.42	20.62	101.46	3.49
6000.000	68.36	1.63	12.45	19.96	42.04	.68
6250.000	75.42	1.74	11.38	19.23	27.36	1.94
6500.000	76.11	2.15	8.77	27.49	52.40	3.62
6750.000	67.16	1.54	13.40	33.09	96.85	3.68
7000.000	72.32	1.36	16.26	40.33	110.83	3.34
7250.000	64.70	2.08	9.12	47.34	-144.02	3.15
7500.000	64.76	1.15	23.24	46.97	-95.86	1.13

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#51 IN-7 OUT-17



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#51 IN-7 OUT-17

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	77.17	1.12	24.74	49.22	-123.52	.70
2750.000	87.63	1.53	13.58	40.76	169.88	.70
3000.000	84.86	1.11	25.43	31.58	110.01	.65
3250.000	82.19	1.12	24.89	23.32	16.76	1.25
3500.000	74.69	1.23	19.77	16.48	-115.05	2.13
3550.000	78.54	1.12	24.96	17.20	147.61	5.39
3600.000	82.30	1.30	17.77	18.21	50.64	5.29
3650.000	73.81	1.41	15.37	19.03	-36.42	4.78
3700.000	64.33	1.43	15.03	18.95	-121.37	4.81
3750.000	76.67	1.11	25.98	18.12	150.37	5.02
3800.000	71.76	1.30	17.61	17.46	58.09	5.33
3850.000	66.65	1.46	14.32	16.78	-41.51	5.46
3900.000	74.83	1.35	16.47	17.85	-139.06	5.23
3950.000	71.12	1.29	17.97	18.84	130.07	4.96
4000.000	65.62	1.28	18.16	20.08	42.20	4.83
4050.000	63.56	1.13	24.22	20.44	-43.73	4.78
4100.000	66.56	1.22	20.22	21.05	-129.75	4.77
4150.000	74.61	1.11	25.47	21.06	144.62	4.76
4200.000	69.25	1.29	18.07	21.92	56.76	4.62
4250.000	60.61	1.29	17.93	21.37	-21.84	4.64
4300.000	59.27	1.12	24.67	20.66	-106.45	4.86
4350.000	69.60	1.12	25.24	20.36	162.33	4.94
4400.000	63.20	1.15	22.87	20.04	73.57	4.98
4450.000	70.31	1.23	19.67	19.86	-17.11	5.00
4500.000	65.74	1.27	18.44	20.03	-106.36	4.93
4550.000	74.90	1.14	23.48	20.09	165.52	4.93
4600.000	63.24	1.12	25.16	20.32	76.06	4.89
4650.000	74.37	1.23	19.80	20.44	-10.66	4.64
4700.000	65.52	1.10	26.79	20.66	-98.05	4.77
4750.000	69.74	1.33	16.96	20.14	177.57	4.68
4800.000	73.07	1.14	23.56	19.93	86.29	4.95
4850.000	73.92	1.06	30.19	20.01	-.77	4.89
4900.000	74.94	1.10	26.41	15.73	-89.64	5.00
4950.000	66.20	1.31	17.35	19.79	179.08	5.00
5000.000	74.47	1.15	23.28	20.34	90.35	4.89
5050.000	63.67	1.22	19.99	20.51	3.08	4.76
5100.000	72.43	1.14	23.43	20.90	-80.95	4.79
5150.000	77.52	1.16	22.41	20.39	-169.26	4.80
5200.000	84.95	1.28	18.11	20.05	106.28	4.86
5250.000	82.62	1.15	23.01	20.17	15.00	4.88
5300.000	73.47	1.17	22.32	19.35	-69.31	5.08
5350.000	75.50	1.36	16.33	19.34	-167.98	5.09
5400.000	79.01	1.26	16.23	19.95	107.63	4.84
5450.000	75.16	1.44	14.60	20.03	17.87	4.87
5500.000	69.85	1.36	16.40	19.95	-67.64	4.60
5550.000	109.09	1.32	17.11	19.90	-157.79	4.99
5600.000	74.70	1.10	26.07	19.98	112.66	4.73
5650.000	71.00	1.32	17.11	19.88	32.08	4.82
5700.000	70.26	1.11	25.56	18.61	-59.99	3.06
5750.000	73.70	1.13	24.31	18.20	-150.17	3.16
5800.000	85.66	1.31	17.43	17.61	112.66	3.31
5850.000	78.10	1.76	11.69	13.02	12.91	5.05
5900.000	75.36	1.74	11.37	15.37	-69.13	5.05
5950.000	78.43	1.92	10.06	17.32	-162.80	5.38
6000.000	74.35	1.63	12.45	17.73	97.34	1.72
6250.000	77.36	1.04	34.39	19.12	11.39	1.13
6500.000	69.63	1.21	20.52	22.49	-105.62	1.25
6750.000	65.15	1.24	19.34	24.94	147.21	1.21
7000.000	73.05	1.53	12.95	37.77	36.62	.61
7250.000	68.11	1.14	23.41	37.96	.09	.33
7500.000	77.66	1.30	17.66	46.67	-112.30	.33

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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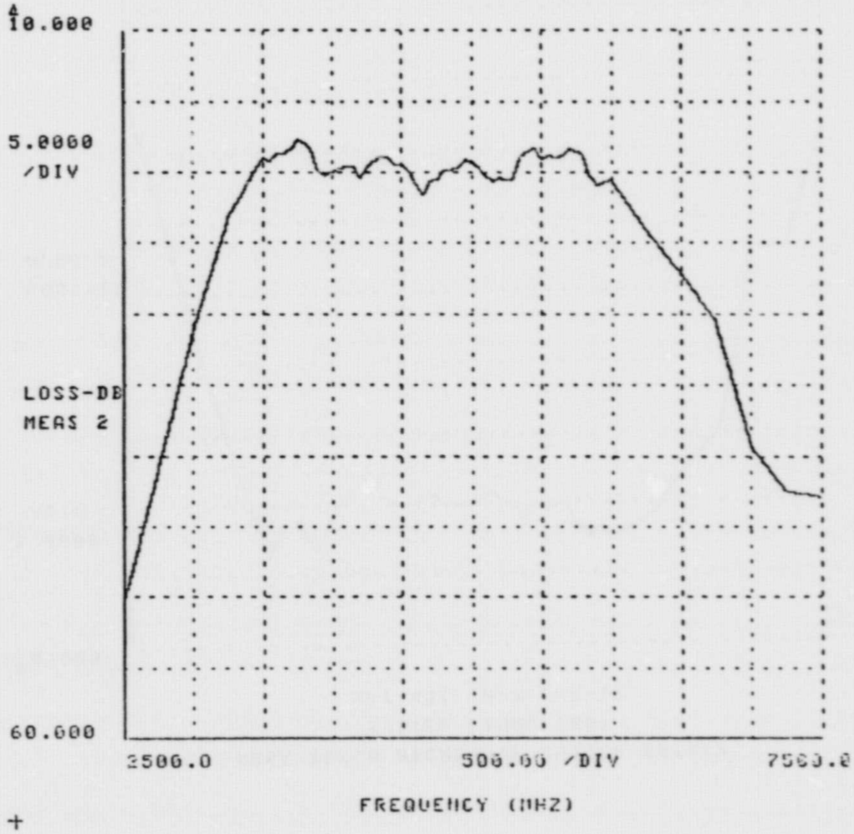
NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#53 IN-11 OUT-17



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OF POOR QUALITY

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#53 IN-11 OUT-17

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTH LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	86.20	1.13	24.46	50.37	110.20	-.01
2750.000	91.79	1.02	40.36	41.03	117.42	-.01
3000.000	64.51	1.35	16.55	31.37	111.75	.29
3250.000	86.79	1.16	22.51	23.18	65.33	.53
3500.000	84.25	1.27	18.41	19.01	16.15	1.22
3550.000	74.31	1.29	18.00	19.15	-66.87	4.51
3600.000	74.49	1.14	23.55	16.73	-146.21	4.44
3650.000	84.10	1.57	13.05	18.69	133.37	4.44
3700.000	74.19	1.60	12.69	18.37	53.90	4.46
3750.000	97.82	1.22	20.05	17.63	-27.36	4.60
3800.000	81.37	1.14	23.52	17.96	-111.56	4.67
3850.000	74.10	1.21	20.33	18.46	164.59	4.47
3900.000	72.86	1.26	18.72	19.95	87.67	4.10
3950.000	69.67	1.09	27.46	20.21	16.84	4.05
4000.000	65.47	1.11	25.70	19.96	-57.96	4.19
4050.000	71.04	1.09	27.00	19.76	-133.86	4.23
4100.000	72.12	1.24	19.52	19.56	149.74	4.34
4150.000	77.47	1.07	29.79	19.55	69.74	4.24
4200.000	75.37	1.37	16.05	20.45	-3.02	4.05
4250.000	80.74	1.27	18.45	19.62	-77.53	4.17
4300.000	75.95	1.16	22.49	19.24	-153.14	4.31
4350.000	77.15	1.07	29.81	16.90	127.13	4.45
4400.000	68.93	1.40	15.54	18.92	46.75	4.40
4450.000	75.62	1.52	13.76	19.49	-31.24	4.28
4500.000	70.42	1.24	19.25	19.53	-107.21	4.29
4550.000	70.47	1.21	20.38	19.87	174.36	4.30
4600.000	63.43	1.49	14.05	20.88	98.04	4.03
4650.000	62.44	1.42	15.26	21.56	29.41	3.85
4700.000	63.89	1.41	15.46	20.68	-40.69	4.11
4750.000	64.19	1.27	18.50	20.46	-118.41	4.22
4800.000	69.53	1.25	19.31	19.92	167.53	4.21
4850.000	73.81	1.13	24.52	19.82	89.93	4.28
4900.000	72.61	1.56	13.21	19.69	13.39	4.28
4950.000	65.82	1.74	11.40	19.10	-64.09	4.42
5000.000	68.84	1.40	15.64	19.34	-145.61	4.40
5050.000	80.05	1.53	13.54	19.62	137.43	4.26
5100.000	78.77	1.47	14.45	20.20	60.19	4.15
5150.000	77.10	1.58	12.91	20.60	-11.96	4.07
5200.000	86.01	1.47	14.36	20.44	-86.26	4.16
5250.000	64.74	1.46	14.54	20.56	-161.64	4.02
5300.000	73.33	1.54	13.43	20.39	120.99	4.07
5350.000	71.77	1.42	15.23	18.63	51.60	4.39
5400.000	78.63	1.50	13.98	18.53	-29.15	4.57
5450.000	73.35	1.56	13.17	18.36	-112.85	4.50
5500.000	76.53	1.31	17.46	19.12	166.92	4.26
5550.000	78.51	1.41	15.42	18.58	93.77	4.34
5600.000	72.52	1.05	32.54	18.90	12.82	4.26
5650.000	78.10	1.24	19.34	18.82	-59.46	4.42
5700.000	74.42	1.33	16.94	18.30	-146.35	4.59
5750.000	75.08	1.54	13.19	13.53	135.30	4.53
5800.000	79.85	1.31	10.77	18.76	59.30	4.61
5850.000	75.41	2.17	8.67	23.29	-30.42	4.25
5900.000	70.50	1.95	9.82	20.92	-102.34	4.15
5950.000	70.28	2.14	8.79	20.66	-175.85	4.34
6000.000	72.88	1.93	19.65	20.57	101.38	1.14
6250.000	67.74	1.51	13.85	24.13	56.59	.36
6500.000	73.17	2.12	8.90	27.13	36.07	.33
6750.000	68.12	1.14	23.90	30.49	-2.50	.33
7000.000	72.20	1.41	13.40	39.43	-13.93	.13
7250.000	67.68	1.82	10.75	42.48	-26.01	.22
7500.000	64.93	1.53	13.34	42.83	-62.79	.22

REF FLANE EXT(CM): INPUT= .00 TRAN= .00

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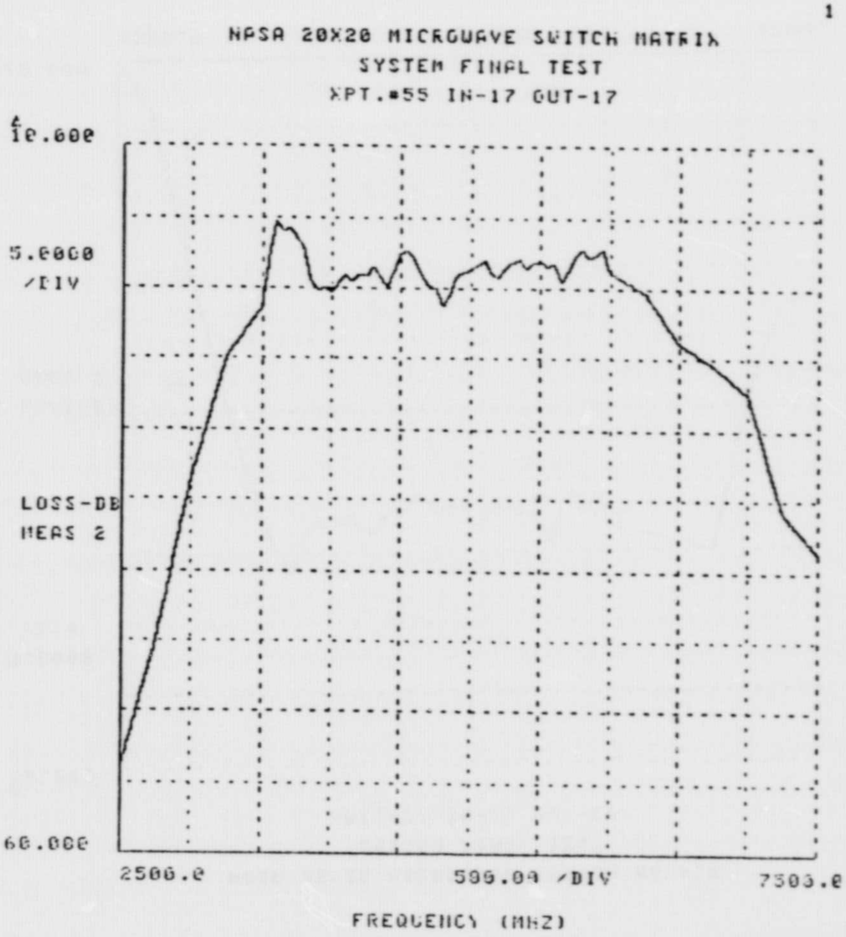

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NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.=55 IN-17 OUT-17

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	83.26	1.20	20.69	53.98	-12.68	.89
2750.000	82.72	1.17	22.30	45.04	96.14	2.89
3000.000	82.01	1.34	16.72	33.65	-172.43	3.15
3250.000	83.09	1.12	24.66	24.80	-111.36	3.37
3500.000	60.55	1.29	17.96	21.36	-56.41	3.26
3550.000	79.13	1.21	20.26	18.08	-105.43	3.57
3600.000	89.04	1.58	13.00	15.32	173.07	4.26
3650.000	78.03	1.82	10.72	15.90	101.06	3.86
3700.000	74.61	1.27	16.61	15.86	34.10	3.73
3750.000	76.19	1.34	16.65	16.49	-33.27	3.65
3800.000	89.50	1.09	27.62	17.09	-97.43	3.51
3850.000	86.67	1.42	15.18	19.59	-159.66	3.00
3900.000	77.63	1.29	16.01	20.18	154.47	2.67
3950.000	84.07	1.20	20.72	19.94	97.02	3.03
4000.000	87.46	1.42	15.15	20.20	45.40	2.98
4050.000	82.83	1.53	13.51	19.60	-10.34	3.17
4100.000	77.51	1.36	16.02	19.03	-66.85	3.26
4150.000	75.64	1.64	12.33	19.52	-127.55	3.12
4200.000	88.09	1.62	12.52	19.02	178.95	3.13
4250.000	74.61	1.38	15.89	19.13	119.61	3.27
4300.000	66.76	1.25	19.11	16.54	61.24	3.27
4350.000	78.33	1.18	21.65	19.22	1.97	3.07
4400.000	68.89	1.20	20.97	19.56	-49.32	2.80
4450.000	74.36	1.42	15.28	18.73	-98.90	3.10
4500.000	70.09	1.77	11.12	17.47	-160.95	3.53
4550.000	74.64	1.62	12.50	17.43	134.02	3.53
4600.000	65.93	1.32	17.15	18.09	71.68	3.32
4650.000	63.39	1.11	25.58	19.15	14.48	3.12
4700.000	88.09	1.24	19.55	19.88	-40.26	2.98
4750.000	60.96	1.21	20.53	19.94	-92.88	2.99
4800.000	74.03	1.47	14.44	21.17	-147.96	2.74
4850.000	70.18	1.46	14.22	20.46	168.60	2.76
4900.000	64.06	1.14	23.66	19.12	112.77	3.22
4950.000	67.14	1.53	13.62	18.86	52.72	3.21
5000.000	72.68	1.72	11.58	18.64	-2.96	3.23
5050.000	67.93	1.38	15.88	18.33	-63.41	3.33
5100.000	67.56	1.46	14.60	18.09	-122.94	3.26
5150.000	66.92	1.24	19.31	19.02	179.39	3.11
5200.000	75.98	1.45	14.65	19.22	125.24	2.93
5250.000	67.44	1.34	16.62	18.44	73.79	3.11
5300.000	71.22	1.30	17.59	18.13	13.14	3.32
5350.000	68.61	1.11	25.44	17.52	-45.65	3.24
5400.000	73.59	1.26	16.92	18.55	-103.40	3.16
5450.000	81.70	1.55	13.37	16.18	-159.24	3.17
5500.000	65.13	1.80	10.86	18.05	142.65	3.27
5550.000	68.41	1.94	9.91	18.42	82.99	3.23
5600.000	69.09	1.56	13.23	16.26	26.38	3.13
5650.000	66.47	1.03	23.52	19.54	-29.61	2.99
5700.000	66.75	1.11	25.64	18.67	-31.23	2.93
5750.000	73.95	1.63	12.44	17.74	-133.98	3.39
5800.000	67.65	2.46	7.48	17.20	136.73	3.49
5850.000	67.14	2.48	7.42	17.79	98.54	3.25
5900.000	69.33	2.27	8.21	17.61	39.61	3.44
5950.000	67.81	2.22	8.43	17.24	-25.21	3.52
6000.000	66.51	1.72	11.54	18.84	-37.90	3.28
6250.000	67.79	1.52	13.73	20.26	-13.90	3.23
6500.000	73.90	1.86	10.42	23.95	31.41	3.18
6750.000	66.73	1.23	19.62	25.42	127.33	3.13
7000.000	68.77	1.63	12.38	27.36	-151.44	3.35
7250.000	71.21	3.27	5.49	33.36	-115.76	3.12
7500.000	64.61	1.24	19.31	38.70	7.13	1.12

REF PLANE EXT(CM): INPUT= .06 TRAN= .00

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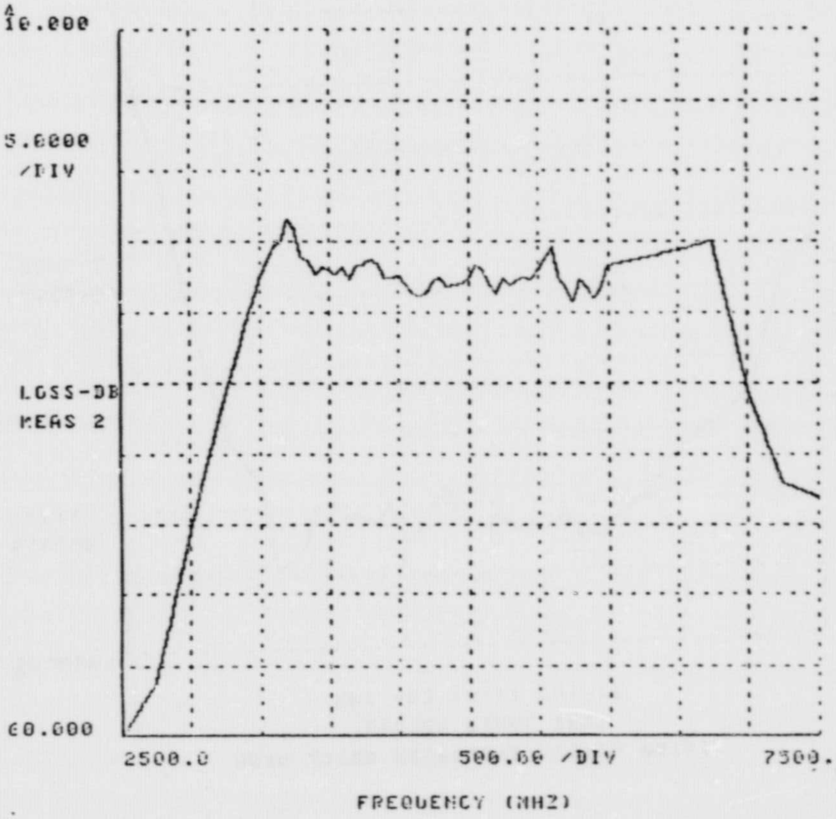
NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#57 IN-21 OUT-17



10-29-82

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#57 IN-21 OUT-17

FREQ-MHZ	ISOL-DB MEAS 1	VSWF MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	87.71	1.27	16.59	64.78	-129.01	.12
2750.000	84.95	1.13	24.37	56.25	42.13	2.12
3000.000	79.60	1.21	20.51	45.59	-151.16	2.35
3250.000	87.22	1.67	30.01	35.79	-20.01	2.66
3500.000	80.66	1.24	19.39	27.66	89.62	2.74
3550.000	91.39	1.17	22.26	26.48	44.33	2.92
3600.000	81.97	1.38	15.86	25.45	-15.52	2.95
3650.000	78.05	1.93	9.97	25.02	-62.00	2.90
3700.000	70.27	1.43	15.06	23.35	-120.00	3.41
3750.000	87.46	1.33	17.04	24.12	175.37	3.00
3800.000	80.75	1.21	20.29	26.07	132.09	2.53
3850.000	77.17	1.41	15.44	26.37	84.13	2.50
3900.000	74.41	1.57	13.11	27.22	42.19	2.42
3950.000	80.16	1.46	14.60	26.81	-2.85	2.52
4000.000	79.49	1.47	14.35	26.97	-48.41	2.46
4050.000	77.22	1.63	12.42	27.31	-91.52	2.45
4100.000	78.35	1.31	17.41	26.77	-136.60	2.53
4150.000	81.50	1.77	11.15	27.63	177.24	2.30
4200.000	71.57	1.69	11.81	26.55	140.45	2.50
4250.000	67.51	1.27	16.46	26.61	87.32	2.71
4300.000	67.47	1.08	28.29	26.19	42.93	2.56
4350.000	70.79	1.20	20.67	26.56	-4.67	2.65
4400.000	72.44	1.50	13.98	27.52	-52.63	2.34
4450.000	83.63	1.24	19.33	27.57	-86.07	2.32
4500.000	65.17	1.02	36.30	27.39	-136.32	2.64
4550.000	65.13	1.24	19.37	27.95	175.94	2.41
4600.000	62.56	1.17	21.90	28.67	136.79	2.13
4650.000	55.16	1.30	17.76	26.88	99.35	2.32
4700.000	65.19	1.15	23.36	28.63	53.19	2.23
4750.000	61.17	1.20	20.83	27.70	18.94	2.44
4800.000	67.02	1.26	18.64	27.56	-34.47	2.61
4850.000	70.03	1.27	18.50	28.24	-75.67	2.25
4900.000	69.35	1.09	27.34	26.03	-115.53	2.33
4950.000	71.50	1.35	16.55	27.96	-158.92	2.37
5000.000	64.34	1.80	10.87	27.63	159.04	2.50
5050.000	68.96	1.61	12.61	26.60	111.04	2.61
5100.000	67.16	1.72	11.50	26.95	65.15	2.62
5150.000	68.61	1.33	16.87	27.54	16.64	2.35
5200.000	77.14	1.66	12.11	28.65	-19.36	2.11
5250.000	82.91	1.56	13.19	27.61	-59.36	2.42
5300.000	65.95	1.24	15.30	26.13	-106.36	2.36
5350.000	68.37	1.11	25.92	27.66	-144.18	2.38
5400.000	75.40	1.09	27.10	27.57	167.65	2.41
5450.000	63.72	1.36	16.30	27.64	129.09	2.29
5500.000	67.40	1.67	12.06	27.02	65.56	2.46
5550.000	66.63	2.06	9.19	26.16	39.78	2.76
5600.000	65.55	1.63	11.95	25.38	-13.70	2.93
5650.000	67.75	1.30	17.51	27.61	-63.93	2.39
5700.000	74.02	1.40	13.51	29.24	-105.84	1.95
5750.000	69.04	1.50	14.03	29.34	-135.19	2.10
5800.000	68.14	1.58	12.98	27.66	177.49	2.56
5850.000	72.06	1.95	9.82	28.21	131.74	2.39
5900.000	69.75	1.79	11.04	29.02	91.38	2.10
5950.000	74.11	1.73	11.47	26.22	55.97	2.18
6000.000	70.99	1.62	12.51	26.62	13.06	2.36
6250.000	71.56	1.74	11.33	25.15	139.11	2.39
6500.000	69.18	2.14	8.78	25.55	-92.39	2.66
6750.000	60.28	1.54	13.40	24.91	20.10	2.73
7000.000	65.10	1.36	16.26	35.69	136.26	2.54
7250.000	63.23	2.07	9.14	42.05	-75.14	2.26
7500.000	67.51	1.15	23.27	43.06	88.73	.26

REF PLANE EXT(CM): INPUT= .00 TRAN= .09

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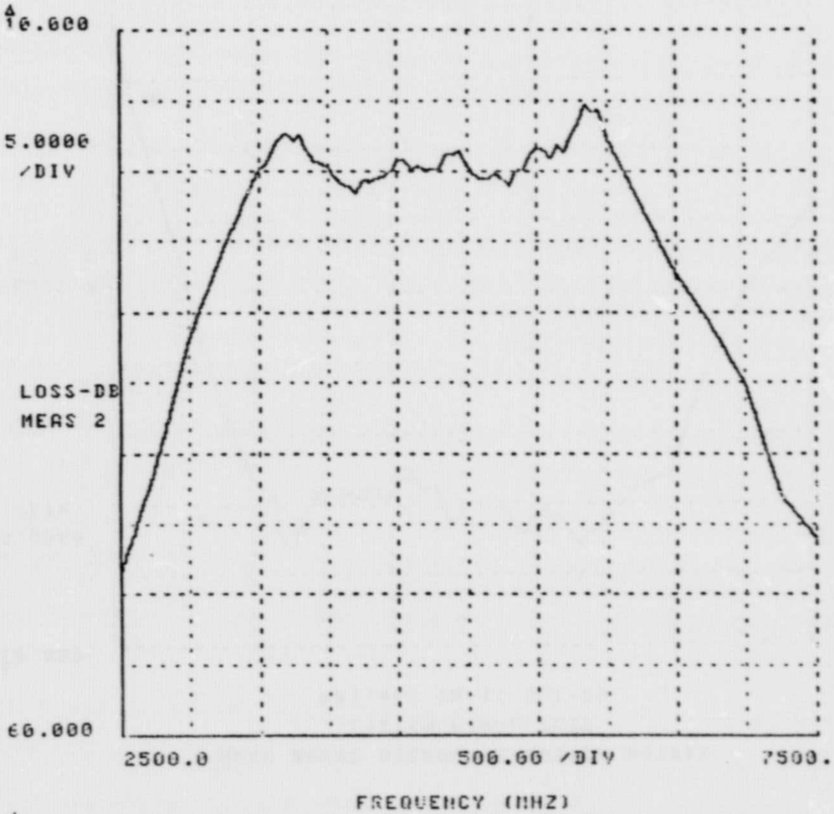
OF POOR QUALITY

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#59 IN-7 OUT-22

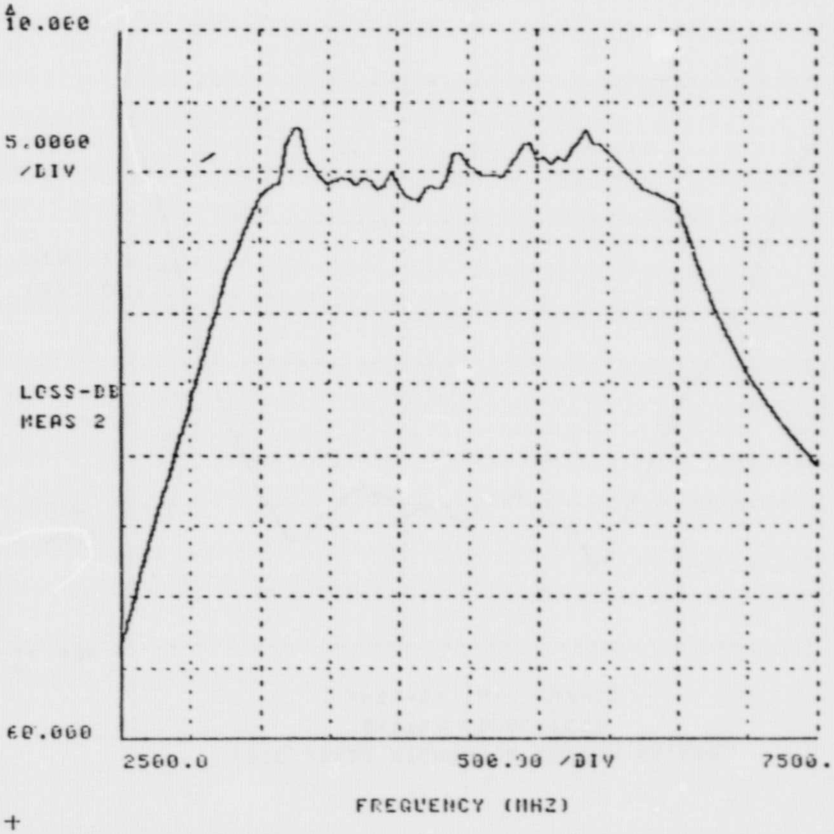


NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#59 IN-7 OUT-22

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	81.72	1.12	24.92	48.53	118.91	1.61
2750.000	84.90	1.53	13.54	41.17	158.18	3.61
3000.000	77.99	1.12	25.17	31.94	-171.25	1.70
3250.000	60.51	1.12	25.62	25.40	-162.45	.01
3500.000	67.35	1.23	19.85	19.88	-173.69	.70
3550.000	66.44	1.12	24.81	19.46	112.79	4.03
3600.000	69.91	1.30	17.62	18.51	41.31	4.12
3650.000	70.40	1.41	15.38	17.68	-35.45	4.29
3700.000	66.79	1.43	15.06	17.35	-113.28	4.26
3750.000	72.45	1.10	26.26	17.85	171.23	4.13
3800.000	68.99	1.30	17.67	17.43	97.99	4.23
3850.000	66.66	1.48	14.22	16.66	18.86	4.03
3900.000	74.63	1.36	16.36	19.31	-46.99	3.75
3950.000	73.78	1.29	17.90	19.47	-116.12	3.88
4000.000	79.71	1.23	18.10	19.73	173.36	3.65
4050.000	76.03	1.13	24.13	20.49	105.35	3.74
4100.000	86.73	1.22	20.16	20.94	38.82	3.65
4150.000	76.64	1.12	24.83	21.00	-26.06	3.62
4200.000	73.43	1.26	18.27	21.49	-91.56	3.61
4250.000	70.85	1.28	18.19	20.59	-155.86	3.66
4300.000	60.26	1.12	25.07	20.72	135.65	3.79
4350.000	65.08	1.11	25.50	20.47	67.72	3.75
4400.000	76.27	1.15	22.92	20.37	.86	3.70
4450.000	67.86	1.23	19.66	20.03	-65.51	3.80
4500.000	76.43	1.28	18.35	19.16	-136.07	3.97
4550.000	67.93	1.14	23.49	19.27	151.54	3.94
4600.000	65.46	1.12	25.27	19.90	82.04	3.79
4650.000	76.23	1.22	19.92	19.62	15.26	3.76
4700.000	70.30	1.10	26.65	19.90	-53.45	3.65
4750.000	67.53	1.34	16.83	19.91	-123.16	3.65
4800.000	66.65	1.15	23.11	19.92	175.21	3.66
4850.000	64.77	1.07	29.09	18.87	105.89	3.99
4900.000	66.54	1.11	25.75	18.77	31.45	4.06
4950.000	69.98	1.33	17.07	18.62	-41.87	3.99
5000.000	66.94	1.15	22.90	19.66	-112.24	3.69
5050.000	67.77	1.23	19.79	20.20	176.12	3.63
5100.000	69.08	1.14	23.60	20.54	117.05	3.59
5150.000	70.73	1.16	22.44	20.49	48.76	3.80
5200.000	76.16	1.29	16.07	20.13	-19.75	3.77
5250.000	71.37	1.16	22.46	20.45	-87.05	3.79
5300.000	78.96	1.17	21.93	21.03	-156.05	3.57
5350.000	73.23	1.35	16.55	20.02	144.41	3.59
5400.000	68.31	1.27	16.50	19.85	74.72	3.87
5450.000	73.57	1.43	15.09	18.87	5.13	3.91
5500.000	74.99	1.34	16.66	18.38	-65.94	4.07
5550.000	87.23	1.32	17.26	18.55	-141.41	3.93
5600.000	73.35	1.10	23.26	19.13	152.47	3.73
5650.000	92.83	1.32	17.11	18.11	83.58	3.82
5700.000	80.47	1.10	26.06	18.69	14.78	3.33
5750.000	87.04	1.13	24.59	17.41	-51.94	3.90
5800.000	75.05	1.31	17.43	16.55	-125.61	4.17
5850.000	79.75	1.72	11.59	13.33	154.90	4.30
5900.000	68.73	1.75	11.30	13.73	72.37	4.49
5950.000	75.32	1.93	9.98	15.70	-6.92	4.54
6000.000	91.56	1.64	12.35	17.48	-91.05	3.96
6250.000	70.25	1.04	35.03	22.44	-74.86	1.94
6500.000	64.27	1.21	29.60	27.29	-83.92	1.87
6750.000	68.16	1.24	19.42	30.84	-52.21	3.71
7000.000	63.23	1.58	12.97	33.16	-29.46	1.84
7250.000	65.49	1.14	23.49	42.98	-24.13	1.72
7500.000	86.19	1.30	17.70	43.99	20.16	1.72

REF PLANE EXT(CM): INPUT= .06 TRAN= .0[illegible]

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#61 IN-11 OUT-22



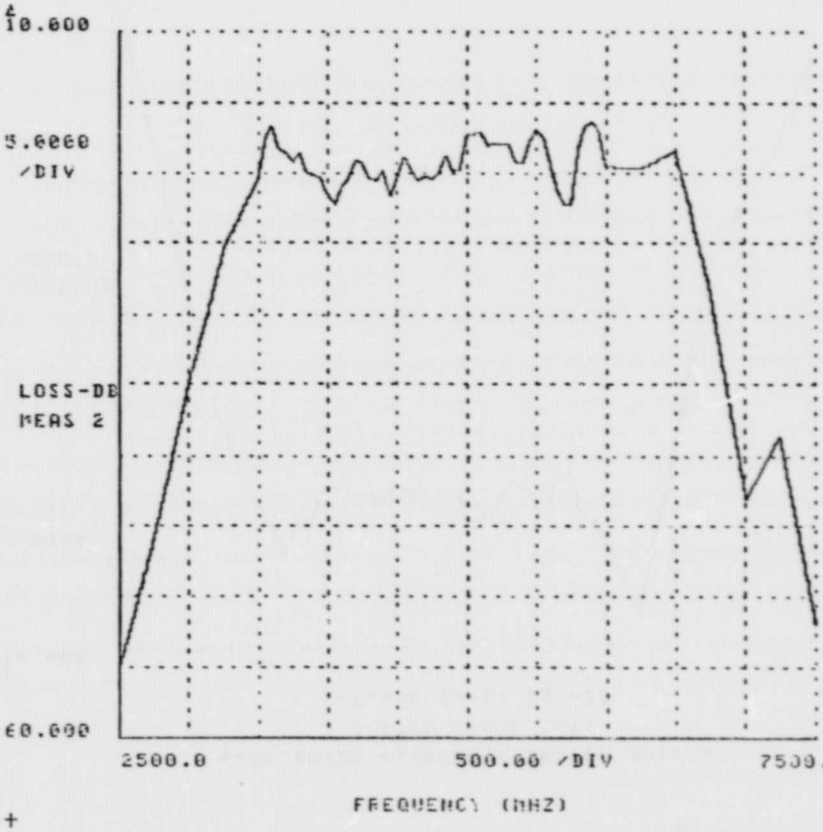
10-29-82

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#61 IN-11 OUT-22

FREQ-MHZ	ISOL-DB MEAS 1	VSWP MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	84.67	1.12	24.77	53.50	-4.11	.84
2750.000	86.30	1.02	41.41	44.59	103.10	2.84
3000.000	78.74	1.35	16.47	36.47	-155.40	3.07
3250.000	76.26	1.16	22.72	27.65	-69.62	3.29
3500.000	75.00	1.27	18.50	21.82	-27.30	3.38
3550.000	69.56	1.27	18.45	21.32	-94.46	3.53
3600.000	71.01	1.13	23.99	20.94	-154.40	3.07
3650.000	71.46	1.59	12.84	20.83	155.16	3.09
3700.000	71.78	1.63	12.37	17.35	94.43	3.76
3750.000	72.69	1.23	19.79	16.89	16.93	4.07
3800.000	72.02	1.13	24.60	16.68	-51.94	3.80
3850.000	70.59	1.21	20.46	19.10	-117.92	3.36
3900.000	61.48	1.26	18.64	19.75	-173.73	3.13
3950.000	74.72	1.09	27.44	20.51	129.42	3.04
4000.000	77.61	1.11	25.33	20.88	76.77	3.01
4050.000	76.05	1.10	26.78	20.58	21.22	3.11
4100.000	72.89	1.23	19.87	20.40	-35.33	3.24
4150.000	72.11	1.06	30.96	20.56	-95.57	3.09
4200.000	72.69	1.37	16.07	20.92	-146.69	3.06
4250.000	76.01	1.28	18.24	20.46	154.28	3.25
4300.000	65.22	1.16	22.60	20.61	96.24	3.17
4350.000	67.73	1.07	29.94	21.28	40.27	2.93
4400.000	70.33	1.40	15.50	20.99	-9.09	3.05
4450.000	73.62	1.52	13.70	20.07	-69.66	3.41
4500.000	77.30	1.25	19.08	20.80	-131.93	3.22
4550.000	88.68	1.21	20.57	21.74	174.57	2.69
4600.000	66.41	1.50	14.02	21.94	123.93	2.80
4650.000	62.37	1.43	15.03	22.63	73.63	2.93
4700.000	65.40	1.43	15.06	21.13	18.45	3.07
4750.000	74.42	1.26	18.75	21.07	-36.91	3.07
4800.000	74.60	1.24	19.48	21.15	-92.23	2.89
4850.000	82.43	1.13	24.16	20.64	-141.04	3.02
4900.000	80.31	1.56	13.26	18.64	159.20	3.49
4950.000	81.51	1.72	11.57	18.74	93.36	3.51
5000.000	72.61	1.41	15.43	19.49	32.69	3.20
5050.000	73.64	1.55	13.34	19.90	-21.91	3.06
5100.000	80.39	1.47	14.49	20.24	-77.32	3.03
5150.000	81.33	1.58	12.94	20.21	-130.90	3.05
5200.000	62.24	1.49	14.12	20.26	172.68	3.00
5250.000	62.83	1.48	14.26	20.34	120.55	2.95
5300.000	78.67	1.54	13.44	19.59	66.62	3.03
5350.000	77.74	1.41	15.39	18.91	11.90	3.26
5400.000	75.45	1.51	13.86	18.07	-56.68	3.53
5450.000	89.17	1.58	13.01	17.93	-115.09	3.36
5500.000	82.07	1.28	18.13	19.19	-171.71	3.14
5550.000	73.56	1.40	15.63	19.03	131.94	3.13
5600.000	72.29	1.05	32.11	19.43	75.50	3.09
5650.000	79.06	1.23	19.36	19.01	29.44	3.06
5700.000	75.79	1.33	16.99	19.18	-34.34	3.10
5750.000	72.73	1.54	13.47	18.43	-91.02	3.21
5800.000	74.74	1.83	10.69	17.79	-150.13	3.46
5850.000	73.80	2.16	8.61	17.01	144.25	3.60
5900.000	71.30	1.94	9.91	18.01	30.16	3.43
5950.000	75.69	2.14	8.79	18.10	21.76	3.33
6000.000	73.70	1.85	10.53	18.53	-39.54	3.23
6250.000	69.59	1.51	13.86	21.21	36.37	3.40
6500.000	60.17	2.12	8.69	22.24	53.31	3.37
6750.000	76.00	1.15	22.95	29.23	150.45	2.90
7000.000	71.64	1.41	15.33	34.27	-92.05	3.10
7250.000	65.84	1.26	10.83	37.83	-46.76	3.04
7500.000	70.33	1.51	13.81	40.73	79.11	1.04

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#63 IN-17 OUT-22



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#63 IN-17 OUT-22

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	90.12	1.20	20.72	55.20	-120.87	1.81
2750.000	87.22	1.17	22.28	45.95	81.45	1.61
3000.000	79.86	1.34	16.73	35.23	-94.39	2.08
3250.000	78.15	1.12	24.67	25.42	66.96	2.27
3500.000	67.94	1.30	17.76	20.42	-143.32	2.31
3550.000	71.88	1.21	20.35	17.67	177.70	2.97
3600.000	73.20	1.59	12.69	16.63	109.91	3.09
3650.000	62.45	1.63	10.66	18.25	66.52	2.36
3700.000	73.16	1.26	16.65	18.53	24.96	2.16
3750.000	70.93	1.34	16.66	19.15	-11.88	2.37
3800.000	72.59	1.08	26.52	18.56	-60.37	2.36
3850.000	70.19	1.41	15.32	19.96	-96.98	2.11
3900.000	73.64	1.29	16.01	20.16	-136.31	2.16
3950.000	65.32	1.20	20.73	20.34	-175.36	2.18
4000.000	77.59	1.43	15.06	21.51	145.26	1.63
4050.000	77.55	1.53	13.52	22.16	116.68	1.64
4100.000	76.04	1.37	16.07	20.92	86.09	1.88
4150.000	86.66	1.63	12.37	20.34	50.64	2.17
4200.000	80.05	1.62	12.54	19.06	7.86	2.42
4250.000	75.23	1.36	15.89	19.24	-36.31	2.31
4300.000	69.54	1.25	19.05	20.34	-75.41	1.97
4350.000	76.56	1.16	21.73	20.49	-107.33	2.05
4400.000	75.62	1.20	20.89	19.75	-149.09	2.15
4450.000	69.61	1.41	15.36	21.60	175.41	1.63
4500.000	66.64	1.77	11.15	20.36	152.26	1.91
4550.000	61.69	1.62	12.52	18.77	106.52	2.51
4600.000	60.91	1.33	17.00	19.62	61.76	2.18
4650.000	62.04	1.12	24.73	20.47	28.21	1.82
4700.000	64.18	1.23	19.88	20.19	-3.61	1.96
4750.000	68.67	1.20	20.75	20.38	-42.31	1.88
4800.000	71.43	1.47	14.44	20.01	-71.40	1.95
4850.000	67.93	1.48	14.22	18.61	-112.50	2.29
4900.000	73.26	1.13	24.54	19.86	-153.76	1.85
4950.000	75.11	1.52	13.65	19.71	-179.00	1.78
5000.000	71.63	1.72	11.56	17.26	142.00	2.35
5050.000	79.62	1.38	15.85	17.25	96.28	2.51
5100.000	69.44	1.46	14.54	17.12	31.79	2.29
5150.000	70.55	1.25	18.94	16.02	13.98	2.06
5200.000	74.69	1.46	14.60	17.87	-22.21	2.16
5250.000	71.67	1.35	16.36	17.91	-63.71	2.21
5300.000	74.51	1.31	17.41	17.85	-101.77	2.17
5350.000	70.51	1.10	26.08	19.13	-141.96	1.94
5400.000	63.47	1.25	19.07	19.22	-171.56	1.76
5450.000	70.99	1.56	13.26	17.72	153.69	2.24
5500.000	75.35	1.82	10.76	16.90	107.81	2.69
5550.000	77.33	1.94	9.90	17.33	57.13	2.59
5600.000	68.92	1.55	13.21	19.22	14.41	2.07
5650.000	67.94	1.08	28.79	21.21	-17.46	1.69
5700.000	67.45	1.12	24.76	22.16	-46.51	1.26
5750.000	64.80	1.64	12.26	22.22	-62.30	1.37
5800.000	61.05	2.48	7.42	18.30	-95.53	2.37
5850.000	59.12	2.47	7.45	16.69	-147.95	2.33
5900.000	58.03	2.24	8.33	16.37	132.00	2.85
5950.000	57.85	2.21	8.46	16.67	109.52	2.74
6000.000	62.51	1.72	11.58	19.53	53.45	1.95
6250.000	69.36	1.52	13.73	19.66	-100.59	2.32
6500.000	65.42	1.85	10.48	18.38	6.66	2.47
6750.000	65.71	1.23	19.71	28.34	174.01	2.18
7000.000	73.68	1.64	12.34	43.10	-25.96	2.29
7250.000	71.71	3.26	5.50	38.52	122.85	1.92
7500.000	74.95	1.25	19.20	51.96	-11.31	1.92

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

10-29-82

NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#65 IN-21 OUT-22

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	79.95	1.27	18.56	57.31	116.07	1.64
2750.000	87.76	1.13	24.37	47.45	40.19	1.04
3000.000	66.57	1.21	20.54	36.43	-70.66	1.41
3250.000	67.60	1.07	29.91	26.23	146.34	1.63
3500.000	74.89	1.24	19.38	20.54	-4.06	1.67
3550.000	74.75	1.16	22.54	20.04	-33.92	1.79
3600.000	66.95	1.38	15.87	18.75	-68.65	1.69
3650.000	74.77	1.93	9.98	18.19	-94.62	1.78
3700.000	95.39	1.43	15.08	16.43	-132.74	2.17
3750.000	77.36	1.32	17.11	17.42	-172.89	2.09
3800.000	69.22	1.21	20.53	16.25	151.66	1.45
3850.000	72.61	1.40	15.48	19.40	134.60	1.48
3900.000	74.22	1.56	13.21	18.54	[illegible]8.53	1.82
3950.000	69.50	1.46	14.64	20.26	[illegible].21	1.36
4000.000	68.51	1.47	14.42	21.13	48.56	1.20
4050.000	69.67	1.63	12.42	21.46	26.09	1.28
4100.000	72.55	1.31	17.46	20.97	2.89	1.20
4150.000	66.77	1.77	11.14	22.11	-17.04	1.13
4200.000	65.11	1.69	11.64	20.25	-37.89	1.41
4250.000	66.10	1.27	18.52	20.17	-67.76	1.65
4300.000	76.34	1.08	28.84	20.36	-97.20	1.41
4350.000	73.59	1.21	20.56	20.78	-118.40	1.32
4400.000	60.24	1.50	13.94	19.79	-144.82	1.54
4450.000	61.43	1.24	19.34	20.50	-173.62	1.31
4500.000	72.60	1.02	38.35	20.86	168.08	1.28
4550.000	72.66	1.24	19.33	20.40	139.98	1.42
4600.000	79.36	1.17	22.01	21.13	116.88	1.32
4650.000	73.18	1.30	17.74	20.26	92.51	1.26
4700.000	77.81	1.14	23.44	21.47	71.41	1.33
4750.000	66.30	1.20	20.81	20.43	44.73	1.29
4800.000	74.37	1.27	16.62	20.52	24.80	1.29
4850.000	72.65	1.27	18.45	20.04	-1.55	1.52
4900.000	63.16	1.09	27.36	19.99	-29.78	1.30
4950.000	74.23	1.35	16.54	20.74	-48.52	1.11
5000.000	72.00	1.80	10.84	19.03	-69.71	1.50
5050.000	83.27	1.62	12.56	18.32	-102.64	1.84
5100.000	99.91	1.73	11.45	18.17	-135.90	1.63
5150.000	89.94	1.34	16.82	19.40	-161.24	1.46
5200.000	78.13	1.66	12.08	19.06	171.53	1.62
5250.000	78.13	1.57	13.14	20.03	140.57	1.39
5300.000	82.30	1.24	19.28	20.93	121.48	1.13
5350.000	76.73	1.11	25.79	21.49	99.72	1.27
5400.000	76.72	1.10	26.70	21.20	75.62	1.13
5450.000	74.17	1.36	16.34	21.77	59.10	1.04
5500.000	65.32	1.66	12.10	20.46	38.16	1.47
5550.000	77.56	2.06	9.22	19.01	6.16	1.87
5600.000	69.49	1.67	12.00	19.03	-29.30	1.60
5650.000	74.48	1.29	17.83	21.29	-51.60	1.22
5700.000	72.29	1.40	15.65	21.77	-73.16	1.07
5750.000	73.39	1.49	14.11	22.07	-90.13	.37
5800.000	82.26	1.58	12.92	20.95	-104.44	1.20
5850.000	71.49	1.95	9.82	19.05	-133.33	1.72
5900.000	66.76	1.78	11.05	18.59	-166.19	1.63
5950.000	72.52	1.73	11.48	16.67	167.95	1.41
6000.000	76.28	1.61	12.63	17.89	142.91	1.93
6250.000	69.07	1.74	11.36	12.31	-40.65	2.13
6500.000	69.77	2.14	8.79	23.07	113.31	1.52
6750.000	63.36	1.54	13.39	35.41	45.64	1.25
7000.000	69.10	1.36	16.23	40.93	-105.36	1.43
7250.000	65.25	2.08	9.12	44.73	144.13	1.01
7500.000	79.29	1.15	23.24	51.26	72.65	1.01

REF PLANE EXT(CM): INPUT= .00 TRAN= .00

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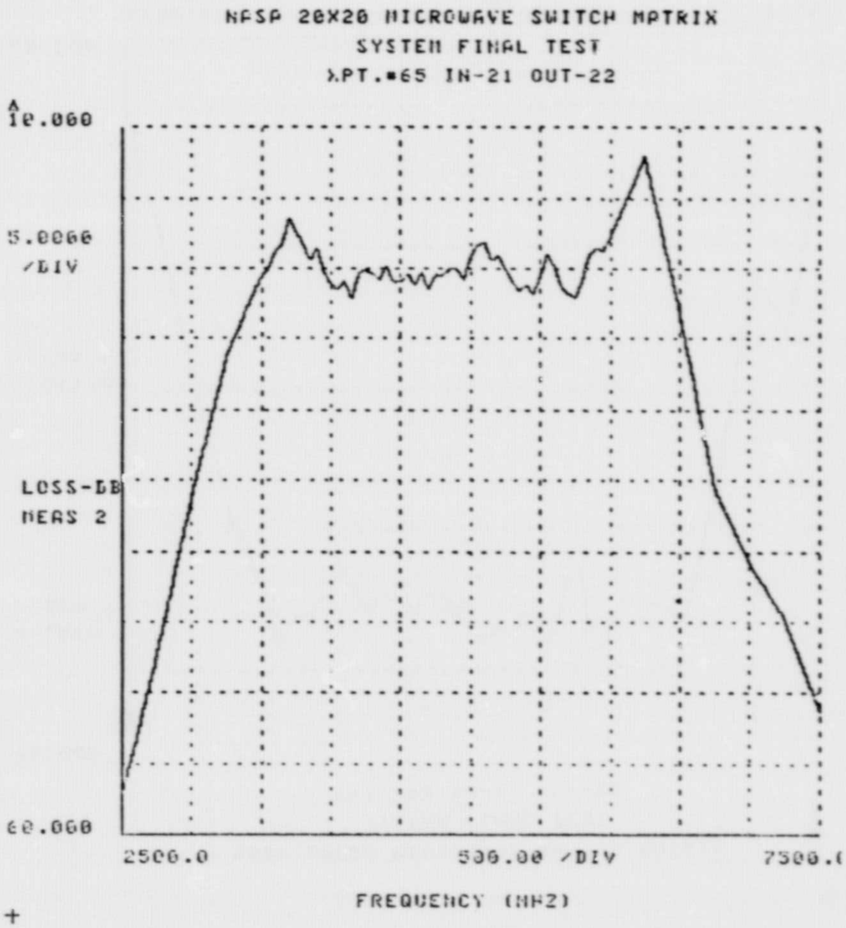
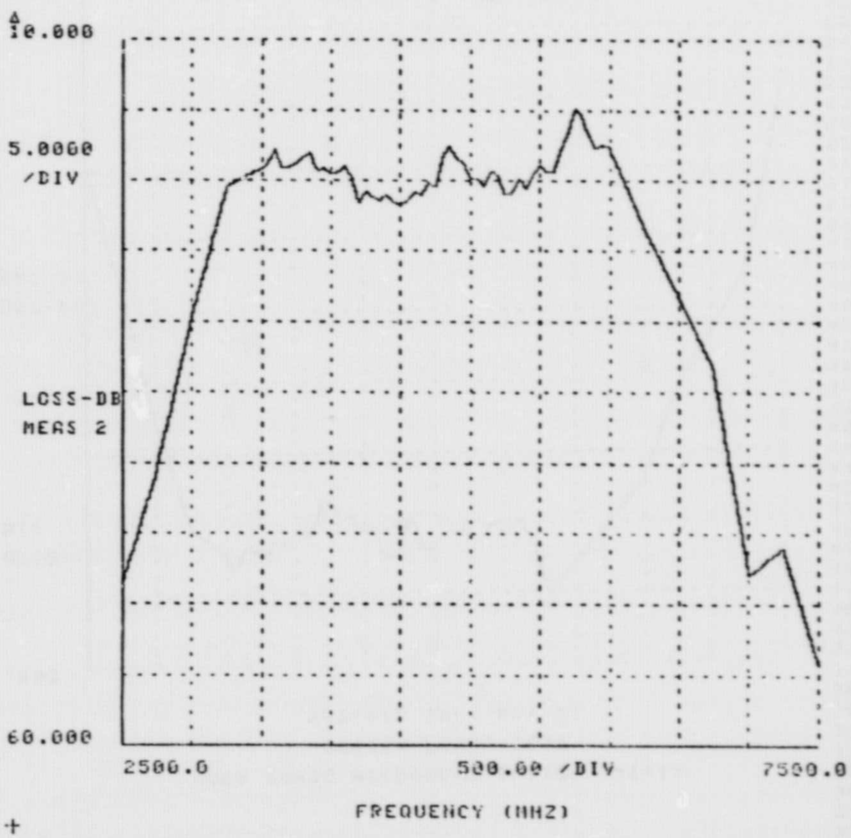


NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#73 IN-1 OUT-17



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#73 IN-1 OUT-17

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	61.30	1.17	22.23	40.59	-125.23	1.74
2750.000	83.08	1.15	23.24	40.55	65.29	1.74
3000.000	81.44	1.37	16.06	29.87	-79.12	2.10
3250.000	88.79	1.04	34.60	20.39	66.12	2.37
3500.000	73.22	1.17	21.09	19.17	-145.87	2.96
3550.000	74.65	1.40	15.53	18.64	106.32	6.56
3600.000	62.59	1.59	12.80	17.80	-22.12	6.47
3650.000	75.86	1.94	9.89	19.14	-126.47	6.00
3700.000	65.27	1.38	15.94	19.04	121.92	6.16
3750.000	82.53	1.19	21.28	16.78	11.22	6.05
3800.000	73.54	1.25	16.99	18.34	-95.74	6.35
3850.000	71.70	1.41	15.31	18.10	142.50	6.40
3900.000	73.38	1.03	37.06	19.32	33.00	6.04
3950.000	82.62	1.17	22.25	19.11	-74.93	6.10
4000.000	70.89	1.14	23.92	19.52	174.43	6.07
4050.000	67.96	1.17	22.14	19.34	66.49	6.10
4100.000	73.29	1.26	18.91	18.99	-45.31	6.38
4150.000	67.34	1.61	12.57	19.85	-163.10	6.05
4200.000	64.60	1.25	19.09	21.56	96.69	5.80
4250.000	61.21	1.31	17.44	20.72	-11.92	5.96
4300.000	61.00	1.12	25.05	21.19	-117.66	5.92
4350.000	66.36	1.07	29.58	21.42	134.69	5.98
4400.000	68.86	1.23	19.61	21.03	27.20	6.03
4450.000	76.76	1.42	15.27	21.57	-82.10	5.93
4500.000	72.98	1.46	14.51	21.66	173.63	5.80
4550.000	70.75	1.08	28.20	21.46	69.07	5.93
4600.000	69.48	1.44	14.66	20.61	-39.62	6.01
4650.000	70.88	1.70	11.76	21.02	-147.43	5.98
4700.000	77.71	1.82	10.76	20.17	105.16	5.92
4750.000	75.53	1.76	11.16	20.43	-.51	5.92
4800.000	67.44	1.73	11.41	18.37	-107.97	6.33
4850.000	76.17	1.37	16.14	17.46	131.53	6.63
4900.000	69.34	1.54	13.50	18.40	13.41	6.37
4950.000	69.94	1.84	10.57	18.69	-97.93	6.16
5000.000	67.60	1.72	11.55	19.83	151.10	6.00
5050.000	71.07	1.47	14.35	19.86	46.10	5.94
5100.000	76.60	1.32	17.27	20.34	-62.56	5.99
5150.000	70.45	1.55	13.35	19.30	-169.42	6.23
5200.000	70.10	1.41	15.47	19.64	73.31	6.31
5250.000	75.91	1.92	10.01	20.91	-36.57	5.73
5300.000	72.50	1.97	5.72	20.78	-133.11	5.93
5350.000	72.17	1.83	10.65	19.81	109.80	6.15
5400.000	73.34	1.59	12.82	20.47	5.60	5.93
5450.000	71.04	1.41	15.31	19.60	-103.52	6.16
5500.000	62.37	1.96	9.77	16.90	143.99	6.28
5550.000	70.47	1.60	12.74	19.34	30.57	6.12
5600.000	78.70	1.26	18.67	19.33	-75.45	5.87
5650.000	80.36	1.41	15.45	17.34	179.26	6.19
5700.000	74.02	1.38	15.92	16.71	60.01	6.33
5750.000	81.33	1.71	11.61	14.93	-57.89	6.29
5800.000	72.82	2.62	6.45	15.31	172.93	6.37
5850.000	72.58	3.45	5.10	16.74	55.11	6.37
5900.000	71.16	3.36	5.33	17.66	-36.31	6.27
5950.000	72.30	2.76	6.59	17.43	-170.49	6.51
6000.000	73.22	1.94	9.94	17.58	69.20	3.23
6250.000	74.31	1.67	12.09	23.43	-159.15	2.28
6500.000	72.43	2.41	7.67	[illegible]	19.49	2.10
6750.000	70.55	1.19	21.57	[illegible]	168.13	2.33
7000.000	74.35	1.63	12.41	47.9[illegible]	-40.27	2.06
7250.000	69.57	1.43	14.96	46.03	133.04	2.14
7500.000	75.31	2.53	7.11	54.23	-33.93	.14

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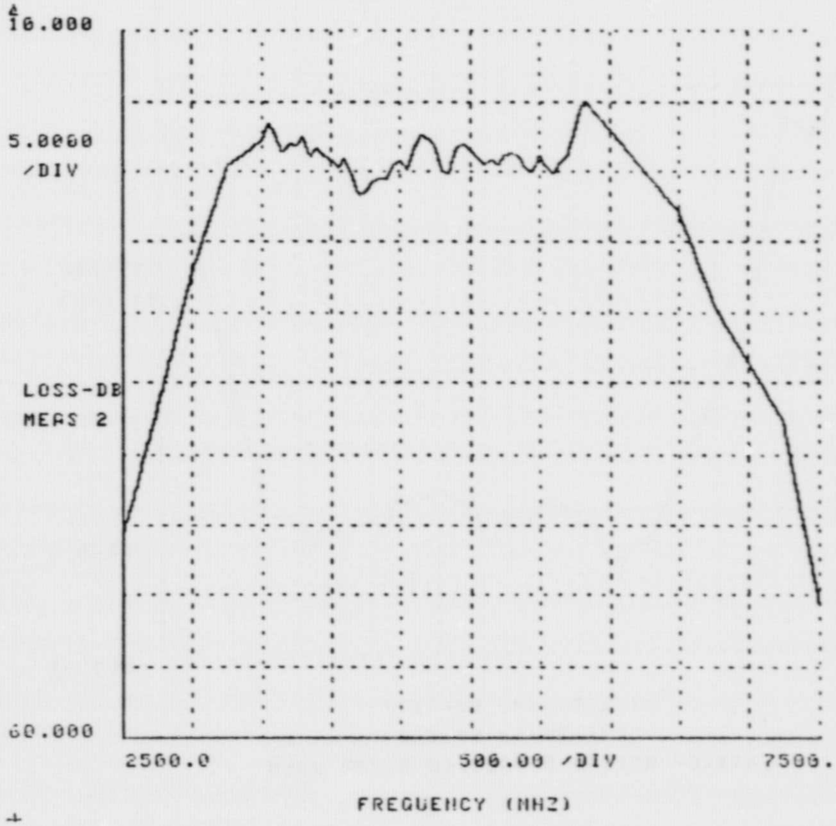
NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#75 IN-1 OUT-22



NASA 20X20 MICROWAVE SWITCH MATRIX
SYSTEM FINAL TEST
XPT.#75 IN-1 OUT-22

FREQ-MHZ	ISOL-DB MEAS 1	VSWR MEAS 2	RTN LOSS MEAS 2	LOSS-DB MEAS 2	PHASE MEAS 2	GP DELAY MEAS 2
2500.000	82.44	1.17	22.23	45.77	147.94	.81
2750.000	84.51	1.15	23.25	36.91	84.36	.81
3000.000	65.72	1.37	16.04	27.34	2.79	1.11
3250.000	86.48	1.04	34.79	19.61	-115.75	1.22
3500.000	72.96	1.17	21.93	17.86	143.91	1.90
3550.000	75.94	1.41	15.46	16.55	39.01	5.86
3600.000	79.04	1.60	12.74	17.36	-66.96	5.15
3650.000	82.17	1.94	9.89	18.62	-146.44	4.78
3700.000	63.39	1.38	15.97	18.07	121.09	5.20
3750.000	82.12	1.19	21.31	16.12	26.17	5.21
3800.000	71.50	1.25	19.01	17.57	-66.32	5.06
3850.000	71.93	1.41	15.35	18.94	-156.06	5.02
3900.000	71.23	1.03	36.89	18.34	113.64	5.09
3950.000	72.95	1.17	22.29	18.67	20.66	5.09
4000.000	75.80	1.14	23.70	19.15	-70.19	4.94
4050.000	77.66	1.17	22.05	19.71	-157.05	4.87
4100.000	90.27	1.25	18.96	19.10	114.58	5.25
4150.000	76.77	1.61	12.64	20.23	14.12	4.69
4200.000	68.29	1.25	19.21	21.68	-61.44	4.46
4250.000	59.52	1.31	17.44	21.49	-146.42	4.71
4300.000	59.68	1.12	24.99	20.70	128.84	4.86
4350.000	58.26	1.07	29.32	20.47	38.03	4.84
4400.000	56.92	1.23	15.69	20.51	-45.26	4.83
4450.000	60.72	1.42	15.24	19.54	-136.03	5.07
4500.000	56.67	1.46	14.52	19.29	132.18	4.92
4550.000	58.59	1.06	28.55	19.81	46.86	4.74
4600.000	55.63	1.45	14.76	18.32	-38.57	5.67
4650.000	60.13	1.70	11.72	17.34	-135.71	5.45
4700.000	60.69	1.82	10.76	17.69	125.19	5.29
4750.000	65.99	1.76	11.21	18.20	33.76	5.10
4800.000	68.11	1.73	11.42	20.05	-58.43	4.61
4850.000	75.26	1.37	16.06	20.11	-132.32	4.58
4900.000	75.54	1.54	13.41	16.38	136.71	5.13
4950.000	81.94	1.85	10.50	17.99	42.87	5.29
5000.000	76.69	1.72	11.53	18.54	-53.66	5.14
5050.000	69.26	1.48	14.34	18.89	-142.09	4.85
5100.000	85.00	1.32	17.27	19.43	131.91	4.97
5150.000	76.91	1.55	13.33	19.15	39.08	4.92
5200.000	78.87	1.41	15.39	19.52	-45.05	4.83
5250.000	72.13	1.93	9.95	16.76	-134.93	5.16
5300.000	82.29	1.97	9.70	18.73	129.86	5.10
5350.000	75.50	1.83	10.65	16.90	41.46	5.07
5400.000	79.14	1.59	12.84	19.75	-53.54	4.89
5450.000	70.69	1.41	15.38	20.04	-134.57	4.77
5500.000	83.44	1.96	9.78	18.87	134.69	5.16
5550.000	82.56	1.60	12.74	19.73	39.79	4.93
5600.000	80.42	1.26	13.71	20.13	-42.93	4.75
5650.000	84.15	1.40	13.48	19.34	-131.33	4.77
5700.000	80.08	1.38	16.01	18.33	145.20	4.34
5750.000	78.05	1.71	11.62	17.14	54.37	3.39
5800.000	79.43	2.83	6.42	15.29	-45.63	3.70
5850.000	75.83	3.45	5.19	15.20	-150.95	5.63
5900.000	73.34	3.37	5.32	15.94	109.22	5.42
5950.000	81.47	2.76	6.58	16.39	13.99	5.37
6000.000	78.81	1.93	9.96	16.99	-83.33	1.87
6250.000	83.41	1.67	12.00	20.03	171.60	1.27
6500.000	81.38	2.41	7.63	22.04	43.56	1.15
6750.000	80.15	1.18	21.55	29.36	-35.66	.31
7000.000	66.74	1.63	12.40	33.62	-115.29	1.15
7250.000	64.45	1.43	14.95	37.73	114.57	1.10
7500.000	60.04	2.58	7.12	50.71	45.02	1.10

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IV. POC MODEL TEST DATA ANALYSIS

1.0 IF FREQUENCY

The IF frequency band was chosen to be 3.5 to 6.0 GHz with a center frequency of 4.75 GHz. This determination was made after an extensive analysis of the worst receive and transmit in-band spurious for an RF input frequency between 27.5 GHz and 30.0 GHz and for an output frequency between 17.7 GHz and 20.2 GHz. The results of this analysis are detailed in the Task 1 report, Sec. 2.3.

2.0 ABSOLUTE MATRIX INSERTION LOSS

The insertion loss of any particular matrix path is determined by the total input and output coupler insertion losses and the corresponding switch amplifier gain. In addition to these individual components, the insertion loss can also vary slightly due to the interactions of these individual components when they are interconnected in the matrix. The theoretical design dictates that if all switch-amplifiers have identical "ON" gain performance and each input-output coupler path pair have the same insertion loss, then the insertion loss for all matrix paths should be the same. In practice, however, there are many fabrication, assembly, and interconnect parameters that will influence the performance of any given path. To help account for these unknown effects, the switch-amplifier design included a final gain adjustment circuit that could help to compensate for insertion loss variations. By varying the bias conditions of the switch-amplifier, the "ON" gain could be adjusted by as much as ± 1.5 dB. This technique provided a large contribution when trying to equalize the matrix path insertion loss. Insertion loss results for the 20 x 20 switch matrix reveal an average insertion loss for all 66

crosspoints of 20.6 dB and a standard deviation of 1.6 dB. This includes only three crosspoints that were off from the average by more than 2.5 dB. Considering the complexity and size of the 20 x 20 switch matrix, these results are quite excellent and that the addition of the bias adjust on the switch-amplifier proved to be a successful technique to help attain these results.

3.0 PASSBAND RIPPLE and BANDWIDTH

The frequency response curves shown earlier in this report reveal the passband ripple of the 20 x 20 switch matrix. The large variations in certain crosspoints are primarily due to the interaction of the long rows of input and output couplers needed in the 20 x 20. This undesirable result was reduced for many crosspoints by doing some alignment in the tray. But for a few crosspoints, alignment proved to be only moderately successful. The general bandwidth for all crosspoints is primarily determined by the bandwidth of the switch-amplifier which is 3.5 GHz to 6.0 GHz, but because of the coupler interaction ripple, the idea of 1 dB or 3 dB bandwidth must be revisited. The frequency response is not simply monotonic so that frequency response roll-off must be differentiated from passband ripple. The basic conclusion of this discussion is that all crosspoints achieved a similar passband roll-off characteristic but certain units exhibited excessive ripple behavior over small sections of the passband. Several crosspoints did, however, achieve the entire 3.5 GHz to 6.0 GHz frequency band with less than 3 dB ripple. Also the specification requiring a 1 GHz bandwidth with less than 1 dB ripple was meet in several crosspoints.

4.0 ISOLATION

The isolation measurement is defined by taking the difference between the "ON" condition insertion loss and the "OFF" condition insertion loss. The signal level strength in the "OFF" condition can be separated into two different components. One component comes from the switch-amplifier "ON" to "OFF" isolation. This has been measured on every individual switch-amplifier prior to matrix integration and found always to exceed 70 dB. The second component can be described as physical isolation between the various microwave circuits. This type of isolation is determined by many factors such as the microwave circuit positioning in the tray as well as the cavities and partitions within the tray. Careful consideration was given to tray design which reduced this type of effect by providing adequate enclosure covers and isolation walls.

The results of the "ON" to "OFF" insertion loss test made on each matrix path were greater than 50 dB. This result tends to support that the dominate component in the isolation measurement is the physical isolation component. Additional tests were carried out using a spectrum analyzer that pointed out additional characteristics of the matrix. If two input signals at two different frequencies are applied to two adjacent input rows and only one crosspoint is turned "ON" a certain amount of the unwanted signal (indicated by the different frequency) will show up at the desired output port. In the worst case measured to date this type of "isolation" was recorded at 40 dB. To help alleviate this type of problem in the future would require better physical isolation of the various microwave circuits.

5.0 VSWR

The input and output VSWR performance is influenced by many different components. The main contributor is the individual couplers themselves - each has an input and coupled port VSWR of between 1.05:1 and 1.4:1 depending on the frequency within the band. Then cascade 22 couplers together for both the input and output divider/combiner networks and the result can be a total VSWR variation of 1.1:1 to 2.0:1. Next add the input and output return loss of each switch-amplifier port compared to the 50 ohm load that is normally present during earlier testing and the VSWR can at some frequencies go as high as 3.0:1 especially in the frequency range from 5.5 GHz to 6.0 GHz. This type of poor VSWR ripple performance can be solved by several different techniques such as improved coupler design and switch-amplifier VSWR and/or the addition of properly placed isolation devices.

6.0 POWER TRANSFER CHARACTERISTICS AND PHASE LINEARITY

The power transfer and phase linearity of the switch matrix is a function of the switch-amplifier performance of these parameters. For the overall 20 x 20 matrix, the 1 dB compression point occurs at an input power level of 15 dBm ± 1 dBm depending on which crosspoint is evaluated. Phase shift at the 1 dB compression point is less than ± 3 degrees and at the 3 dB back-off is less than ± 1 degree. Unless input power level requirements begin to approach the +15 dBm level, there should be no difficulty in meeting standard linearity specifications. In addition, the maximum allowable input power level for the 20 x 20 matrix should not exceed +25 dBm at any time to insure matrix survival.

7.0. SWITCHING SPEED CHARACTERISTICS

The switching speed characteristic was measured on a sample of matrix crosspoints. The results show that the "ON" to "OFF" switching time was less than 10 nsec and usually about 6 nsec. The "OFF" to "ON" switching time was also less than 10 nsec and usually around 4 to 7 nsec. In all cases, the measured switching speed for either "ON" to "OFF" or "OFF" to "ON" will meet the 10 nsec requirement. Switching speed performance could be further improved by reducing the added capacitance used on each control gate of the dual-gate FET switching device. One other approach would be to improve the switching speed characteristics of the switch-driver circuit.

8.0 RECONFIGURATION RATE TESTS

Many tests were performed to demonstrate the many possible matrix state configurations. These tests included such examples as turning on one crosspoint for a pre-set time period and then turning on a different crosspoint after a certain amount of dead time where no crosspoints were on. Other such examples involved several different crosspoints and many different state duration times. Tests were also performed to detail the signal propagation delay time variation when one crosspoint is turned off and another different path length crosspoint is turned on. All crosspoints will change state at the same time if the data transfer pulse electrical length is varied according to the position of each crosspoint within the matrix. To eliminate this problem in the redundant paths is more complex and would require delaying the data transfer pulse at the DCU in some fashion. Without these types of improvements the worst case is a

delay time of 15 nsec for a redundant path.

9.0 ROUTING TESTS

All primary and redundant paths were tested and found to provide 100% operation. In addition, several broadcast mode configurations were tested and the results are presented in the final matrix data section.

V. CRITICAL ASSESSMENTS AND RECOMMENDATIONS

V. CRITICAL ASSESSMENTS AND RECOMMENDATIONS

Although the POC model achieved or exceeded all the required specifications for the 20 x 20 switch matrix, there are several areas where changes could improve performance and/or reduce assembly complexity and integration time.

1.0 ELECTRICAL DESIGN

The electrical design for the 20 x 20 POC model was based on experience gained from the 4 x 4 breadboard switch matrix. Except for improvements in each individual component, no new design concepts were implemented in the 20 x 20 POC model. To improve the matrix performance further will involve not only reviewing each component but also investigating the matrix sub-assemblies as well.

1.1 Coupler

As mentioned earlier in Section I, the long rows of couplers posed certain problems in the 20 x 20 POC model. Although each coupler, when tested individually, provided a satisfactory performance, the interaction of the multi-coupler rows exhibit unpredictable results. The band edge VSWR performance was often a problem as well as the in-band insertion loss ripple. To eliminate these problems, two solutions are possible. One is to improve the individual performance of each individual coupler by incorporating a different design such as a three-section coupler where the bandwidth is wider and the passband performance is more evenly distributed across the band. The second approach is to incorporate isolation devices such as ferrite

isolators at various positions along the coupler chain. This technique would isolate smaller sections of couplers; for example four to six couplers in each section so that the interaction within a 22 coupler row could be controlled. FACC sponsored research and development programs are currently investigating both of these concepts.

1.2 Switch-Amplifier

The switch-amplifier design used in the 20 x 20 POC model performed quite well and required little initial tuning. The major design improvement that could be incorporated combines the driver switching circuit with the switch-amplifier. This improvement could not only reduce the matrix complexity (discused later in Section 2.0), but would also reduce the interconnect parasitics between the current driver and switch-amplifier. Tighter control over these parameters should yield a combined switch-amplifier and driver circuit that performs in a more consistent fashion with respect to passband performance and switching speed. Other possible improvements to the switch amplifier could include a fixed attenuator at the output as well as at the input to improve the output VSWR of the amplifier in both the "ON" and "OFF" switch positions. Also an improved bias control could be incorporated so that each individual device could be set to its optimum bias condition. Improvements associated with the switch-amplifier mechanical integrity must also be addressed especially with respect to the 50 ohm RF feedthrus and the hermetic sealing of the module.

1.3 Switch-Driver

The existing thick-film switch driver circuit worked quite well and presented no performance problems on the 20 x 20 POC model switch matrix. The main area of improvement, as mentioned in the previous paragraph, would be to incorporate this circuit with the switch-amplifier. This would involve converting the thick-film hybrid circuit into a thin- film MIC type circuit. This conversion should not introduce any real problems. One other area of driver improvement could be utilized is a CMOS flip-flop instead of the bipolar type currently being used. This would greatly reduce the driver circuit DC power consumption since each flip-flop would use DC power whether the associated crosspoint is "ON" or "OFF". The major question yet to be answered on the CMOS flip-flop concerns its radiation hardness characteristics.

1.4 Distribution Control Unit

The distribution control unit (DCU) as designed was primarily intended to serve as a testing system for use in the TDMA characterization of the microwave switch matrix. The DCU performed in an excellent fashion by demonstrating the SS-TDMA switching characteristics of the 20 x 20 POC model matrix. No major problems were encountered and no additional design changes are necessary. One topic that was investigated during the program was to use a desk-top computer controller, with the proper interfacing hardware, to simplify the RAM programming of the microwave switch matrix. This option was not implemented due to the increased cost over the manual loading type system.

2.0 MECHANICAL DESIGN

The mechanical design concept used in the 20 x 20 POC model switch matrix provided a flight quality package for the switch matrix. The package design was optimized for small size and low weight, and also included the ability to do final alignment of various critical circuits at the final chassis level. The mechanical designs for individual components such as the switch-amplifier module and switch-driver module were also adequate. Overall the total mechanical packaging concept was very good even though the complexity of the unit due to the large matrix size made certain assembly and rework tasks difficult.

In the switch-amplifier assessment above, the idea of incorporating the switch-amplifier and switch-driver circuits together was suggested. This idea can provide dramatic improvements in the overall mechanical design of a microwave switch matrix. The first improvement would be an obvious parts reduction by implementing this idea. For every two module sets now used, only one would be required. Another important aspect is that the signal and bias routing PC boards could be installed on the same chassis side as the switch-amplifier-driver circuit. This technique eliminates the need for DC feedthrus in the tray and reduces the total number of DC interconnects required. This design approach will also provide access to the output coupler rows on the bottom side of each tray where now the driver circuit boards make it difficult to repair or replace any bottom side couplers. All of this should also have a positive effect on the matrix weight as well.

Other mechanical modifications may also be needed to help incorporate some of the electrical design ideas mentioned earlier. For example,

the use of isolators in the coupler chain may be required and would impact the current chassis design. Also cavity isolation may also need to be improved requiring more tray redesign. The switch-amplifier-driver module must also be improved to yield a stronger physical package with improved assembly procedures.

VI. SWITCH MATRIX RELIABILTY ASSESSMENT

SECTION 6

SWITCH MATRIX RELIABILITY ASSESMENT

1.0 INTRODUCTION

This report discusses the reliability analyses which have been completed for the 20 x 20 IF Switch Matrix. The reliability analyses include reliability assessment, failure modes and effects analysis, circuit stress analysis, and design recommendations.

2.0 TEST AND ANALYSIS PLAN (Subtask 2.8.1)

The reliability of the switch matrix is heavily dependent upon the reliability of the individual switch-amplifier and switch-driver circuits.

The failure rates for all components except for the Raytheon RDX832 GaAs FETs are known with a fairly high degree of certainty and additional testing to verify MIL-HDBK-217C estimates is not justified. However, the failure rate for the FETs is not known with any certainty. These devices have not accumulated sufficient experience either specifically or generically to establish a failure rate with a high degree of confidence.

Initial stress step testing has begun at Raytheon. This initial testing indicates that the activation energy for the RDX832 device appears to be similar to other Raytheon devices. This implies MTTFs of the same order of magnitude as other Raytheon devices. The principal reason for this testing is to establish an accurate value of MTTF for the RDX832 Dual-gate FET being used in this program.

Findings at this time are very preliminary and are not sufficient for considering the device qualified without additional step stress testing.

2.1 RELIABILITY ASSESSMENT

A preliminary reliability assessment for the 20 x 20 matrix was completed in the Task I report and updated for the Task VIII report. Many of the assumptions given in the earlier reports are still unchanged. In this report, an assessment has also been made for the POC model which uses lower reliability components. The POC model as a result has a lower probability of successfully operating than a unit using flight qualified parts. Additional components may also be incorporated in a flight unit to provide additional protection against single point failure modes as discussed in the Task I report or for aging and temperature compensation.

The failure rate assessments for the components in the switch amplifier and the switch driver are shown below:

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IF SWITCH - AMPLIFIER FAILURE RATE

Parts	Quantity	Flight Model Failure Rate $\times 10^{-9}$	POC Model Failure Rate $\times 10^{-9}$
GaAs FETs	2	9.24	462
Thin Film Resistors	9	0.05	0.50
Capacitors (MOM)	11	0.04	0.40
TOTAL		19.37×10^{-9}	932.90×10^{-9}

DRIVER TRANSISTOR FAILURE RATE

Parts	Quantity	Flight Model Failure Rate $\times 10^{-9}$	POC Model Failure Rate $\times 10^{-9}$
Resistors	11	0.05	0.50
Transistor	2	0.70	35
Capacitor, Ceramic	6	0.075	0.75
Integrated Circuit	1	2.5	87.5
TOTAL		4.9×10^{-9}	167.5×10^{-9}

2.2 CROSSPOINT FAILURE RATE

The total failure rate for the crosspoint design is the sum of the RF portion and approximately one-half of the switch driver circuit. Each switch driver controls two crosspoints. The failure of the common integrated circuit could possibly result in the failure of two switches. A short of either one of the driver transistors would result in hard closure of a switch.

Crosspoint Failure Rate (Flight)	21.82×10^{-9}
Crosspoint Failure Rate (POC Model)	1016.65×10^{-9}

2.3 PROBABILITY OF NO OPEN CROSSPOINTS WHICH CAN FAIL THE MATRIX

The development of an exact model of open crosspoints for a generalized switch matrix has been attempted. Unfortunately, it has not been possible to successfully develop either an exact mathematical model nor a cost effective simulation model. Exact math models can be developed for simple matrix sizes (for example, a 4x4 with a wraparound), however, as the matrix size increases the modeling becomes increasingly more complex. The open crosspoint model shown for the 20x20 switch matrix is only a first order approximation. It does not include all possible success states and therefore provides a conservative result.

The probability that there are no open crosspoints which can fail in 10 years can be calculated using the following equations:

Definitions:

$N = 20$, number of rows or columns in the basic matrix excluding redundant wraparound rows or columns.

R = 0.998090 (flight) and 0.914792 (POC model), the reliability of a single crosspoint switch and driver.

W = 0.996184 (flight) and 0.836844 (POC model), the probability that two crosspoints in the redundant wraparound will function.

C = combinatorial expression, $C_i^n = \dfrac{n!}{i! \times (n-i)\,!}$

X = 2, number of redundant wraparound rows or columns

The probability of no open crosspoints failures in the matrix which could disable it can be found by adding the following success path equations:

(1) All crosspoints in the matrix operate without failure

$$R^{N^2}\left(\sum_{i=0}^{84} C_i^{84} \times W^{(84-i)} \times (1-W)^i\right) = R^{N^2}$$

(2) One Failure

$$C_1^{N^2} \times R^{N^2-1} \times (1-R) \times (2W-W^2)$$

(3) Two or more failures in the same column. (Since only one switch is allowed to function at any given time in a column as many as 20 failures can be tolerated as long as the corresponding wrap around switches function).

$$C_1^N \left(\sum_{i=2}^{N} C_i^N \, . \, R^{N^2-i} \quad . \quad (1-R)^i \, . \, (2W-W^2)\, i\right)$$

(4) Two or more failures in the same row. (If more than one switch is turned on in a row as in the broadcast mode. One wraparound column switch and corresponding wraparound row switches will provide the required backup).

$$C^N_1 \left(\mathop{}_{i=2}^{N} C^N_i \; R^{N^2-i} \; (1-R)^i \; (2W^{1/2}-W)\,W^{i/2} \right)$$

(5) Two failures in different rows and columns. (Since two redundant wraparound rows and columns are used, no more than 2 failures can be assumed.)

$$C^N_1 \cdot \left(\mathop{}_{i=1}^{N-1} (N-1)\;(N-i)\; R^{N^2-2}\;(1-R)^2\;(2W^2-(W^2)^2) \right)$$

Evaluating these expressions for 10 years leads to:

	Flight Model	POC Model
(1)	0.465459	—
(2)	0.356286	--
(3)	0.006560	--
(4)	0.006520	--
(5)	0.121201	—
Total	0.956026	0.000000 (P_A)

POC MODEL

The 20 x 20 POC model switch matrix has an estimated probability of zero for successfully operating for 10 years with 484 crosspoints. The calculated reliability of the switch matrix is highly sensitive to the estimated reliability of the individual crosspoints. The POC

model is using much lower quality components than would be used in an actual flight model. At this time, the actual failure rate for the GaAs FETs is the greatest unknown. It is believed that the reliability estimate (based on MIL-HDBK-217C) is probably highly pessimistic for the POC model.

The actual POC model will not be a completely populated 20 x 20 matrix. It will instead consist of only 76 of the 484 possible crosspoints that would be in the complete matrix. The MTBF for the reduced model is estimated to be 12,942 hours, or less than 1 crosspoint failure per year. Two or more GaAs FET failures in the partially populated POC model during a one-year demonstration period would be of concern since it may indicate a higher failure rate for the flight model crosspoint than current estimates.

2.4 PROBABILITY OF NO SHORTED CROSSPOINTS OR MATRIX SHORTS

The following failure modes have been identified which would result in shorted crosspoints:

1) Resistors R4 or R5 in the switch driver (Figure 3.1) failing open.

   (P_1 = 0.999991/0.999912)

2) A collector to emitter short of Q1A or Q1B in the driver.

   (P_2 = 0.999969/0.998468)

3) An open of the -5 V pin in the driver circuit.

   (P_3 = 0.999999/0.999999)

4) An IC Failure. (P_4 = 0.999891/0.996175)

5) Both FETs in a switch amplifier shorting.

(P_5 = 1.0/0.999599).

The probability that a crosspoint short will not occur in the matrix becomes

$$P_B = P_1^{484} \cdot P_2^{484} \cdot P_3^{242} \cdot P_4^{242} \cdot P_5^{484}$$

= 0.955060 (Flight)

= 0.148608 (POC)

The following additional failure modes would result in a catastrophic matrix short:

6) An internal short of the IC or circuit board problem.

(P_6 = 0.999989/0.999617)

7) A short of C5 in the switch amplifier (Figure 3.2)

(P_7 = 0.999998/0.999982)

8) A short of C11 in the switch amplifier

(P_8 = 0.999998/0.999982)

The probability of no disabling matrix short is estimated to be

$$P_C = P_6^{242} \cdot (P_7 \cdot P_8)^{484} = 0.995412 \text{ (Flight)}$$

= 0.895720 (POC)

The probability of no crosspoint shorts and no disabling matrix shorts is estimated to be 0.729570 for the 76 crosspoint POC model.

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2.5 MATRIX RELIABILITY

The reliability of the entire matrix for 10 years is the product of no disabling open crosspoints, no shorted crosspoints, and no disabling circuit shorts:

$P_A \cdot P_B \cdot P_C = 0.908873$ (Flight)

These results are considered pessimistic since it is expected that actual failure rates may be lower than estimated and the modeling of open crosspoints is conservative.

The failure rate of the GaAs FETs is the greatest unknown and demonstration testing of flight representative devices would be required to improve the confidence in the above calculations.

2.6 DISTRIBUTION CONTROL UNIT RELIABILITY

Reliability estimates given in the Task I report for the distribution control unit are basically unchanged. The overall reliability of the controller is dependent upon the type of memory devices which can be used for flight applications. The selection of memory chips is primarily determined by chip susceptibility to total radiation dose as well as susceptibility to soft errors due to cosmic rays.

Two distribution control unit designs have been investigated. The first approach provides for full capability by allowing for any input to be connected to any output. This approach requires approximately 250 1K memory devices and an additional 100 support devices. The estimated reliability for this approach is

1K memory devices	$250 \times 13.7 \times 10^{-9}$
Support devices	$100 \times 9.6 \times 10^{-9}$

TOTAL	4385×10^{-9}

P_S (10 years) = 0.6810

An alternate design consists of a decoder which provides a limited number of switching possibilities. This approach requires a much smaller number of devices, 68 1K memory devices and 120 support devices. The reliability estimate is:

1K memory devices	68 x 13.7
Support devices	120 x 9.6
TOTAL	2084×10^{-9}

P_S (10 years) = 0.8331

2.7 IF SWITCH MATRIX SYSTEM RELIABILITY

The probability of success of the flight model IF Switch Matrix System using a redundant Distribution Control Unit is given by:

$$P_S = 0.908873 \times (1-(1-.8331)^2) = 0.8836 \quad \text{(Flight)}$$

3.0 FALURE MODES AND EFFECTS ANALYSIS

A failure modes and effects analysis has been completed for the switch driver and the switch amplifier. The results are summarized below. An asterisk is placed by circuit references in which a failure results in a permanently closed crosspoint switch or a disabling matrix short. Schematics are given in Figures 3.1 and 3.2 for reference purposes.

SWITCH-DRIVER FMEA (Figure 3.1)

Part	Failure Mode	Effect
C1	Short	No effect.
	Open	Slightly degraded performance when switch is ON.
C2	Short	No effect.
	Open	Slightly degraded performance when switch is ON.
C3	Short	No effect.
	Open	Slightly degraded performance when switch is ON.
C4	Short	No effect.
	Open	Slightly degraded performance when switch is ON.
C5	Short	Degraded Switch A performance, longer response time.
	Open	Overstress of Switch A GaAs FETs possibly resulting in premature failure.
C6	Short	Degraded Switch B performance, longer response time.
	Open	Overstress of Switch B GaAs FETs possibly resulting in premature failure.
R1	Open	Overstress of crosspoint Switch A FETs, possibly resulting in premature failure.
R2	Open	Crosspoint Switch A permanently Open
R3	Open	Crosspoint Switch A permanently Open
R4*	Open	Crosspoint Switch A permanently ON
R5*	Open	Crosspoint Switch B permanently ON.
R6	Open	Overstress of crosspoint Switch B FETs, possibly resulting in premature failure.

R7	Open	Crosspoint Switch B permanently open.
R8	Open	Crosspoint Switch B permanently open.
R9	Open	Degraded Switch A performance, longer response time.
R10	Open	Degraded Switch B performance, longer response time.
R11	Open	Possible false turn-ons and turn-offs of crosspoint Switches A and B.
Q1A*	CE Short	Crosspoint Switch A permanently ON.
	B/E/C Open	Crosspoint Switch A permanently OFF.
Q1B*	CE Short	Crosspoint Switch B permanently ON.
	B/E/C Open	Crosspoint Switch B permanently OFF.
+5V Pin	Open	Crosspoint Switches A and B permanently OFF.
-5V PIN*	Open	Crosspoint Switches A and B permanently ON.
U1-2*	Open	Crosspoint Switch A ON, may go OFF randomly.
-12*	Open	Crosspoint Switch B ON, may go OFF randomly.
-14	Open	Crosspoint Switches A and B permanently OFF.
-7	Open	Crosspoint Switches A and B permanently OFF.
-3*	Open	Crosspoint Switch A permanently ON or OFF.
-11*	Open	Crosspoint Switch B permanently ON or OFF.
-6	Open	Crosspoint Switch A permanently OFF.
-6*	Stuck low	Crosspoint Switch A permanently ON.

-8	Open	Crosspoing Switch B permanently OFF.
-8*	Stuck Low	Crosspoint Switch B permanently ON.
-14/7*	Internal Short	5 volt short may result in loss of matrix.

SWITCH AMPLIFIER FMEA (Figure 3.2)

Part	Failure Mode	Effect
R1	Open	Switch degradation, excessive VSWR.
R2	Open	Loss of RF input, switch permanently open.
R3	Open	Switch degradation, excessive VSWR.
R4	Open	Excessive gain, eventual switch failure.
R5	Open	Excessive gain, eventual switch failure.
R6	Open	Excessive gain, eventual switch failure.
R7	Open	Excessive gain, eventual switch failure.
R8	Open	Q1 permanently ON, reduced isolation.
R9	Open	Q2 permanently ON, reduced isolation.
+5 V pin	Open	Switch permanently OFF.
-5 V pin	Open	Excessive gain, eventual failure.
C1	Open	Switch permanently OFF (open).
	Short	Excessive gain, eventual open switch failure.
C2	Open	Possible noisy operation associated with Q1.
	Short	No effect.
C3	Open	Switch degradation in "ON" state.
	Short	Excessive gain, eventual open switch failure.
C4	Open	Switch degradation in "ON" state
	Short	Excessive gain, eventual open switch failure.
C5	Open	Switch degradation in "ON" state.
*	Short	+5 volt short, loss of matrix.

C6	Open	Switch permanently OFF (open).
	Short	Q2 open, Switch permanently OFF (open).
C7	Open	Switch degradation in "ON" state.
	Short	Excessive gain, eventual open switch failure.
C8	Open	Switch degradation in "ON" state
	Short	Excessive gain, eventual open switch failure.
C9	Open	Switch degradation in "ON" state
	Short	Q2 permanently ON, reduced switch isolation.
C10	Open	Switch permanently open.
	Short	Loss of a single crosspoint, bonding wire fuses open.
C11	Open	Switch degradation in "ON" state
*	Short	+5V short, loss of matrix.
Q1	Open	Switch permanently OFF (open)
	Short	Loss of a single crosspoint, (bonding wire will fuse open)
Q2	Open	Switch permanently OFF (open).
	Short	Loss of a single crosspoint (bonding wire will fuse open).

3.1 CIRCUIT STRESS ANALYSIS

The Switch Driver and the Switch Amplifier have been reviewed for acceptability of part application and stress derating.

3.1.1 SWITCH DRIVER CIRCUIT ANALYSIS

The switch driver uses four component types in its design; deposited resistors, ceramic capacitors, MM4049 transistors, and a 54LS74 integrated circuit. The thin film deposited resistors are well within the FACC derating criteria of no more than 1500 volts per linear inch and 100 watts per square inch of resistor area. The four capacitors which are used for input voltage filtering are stressed at only 10% of their 50 volt rating. Two capacitors are stressed at 5% of their rated 100 V rating. The temperature rise for the capacitors is less than 5° C.

Two high speed transistors are used to drive the crosspoint FETs. The power dissipation for the transistors is 5% of rated with a T_j of 12° C. All secondary stresses are acceptably derated. The fanout on the integrated circuit 54LS74 is 75% of manufacturer's rating versus a 80% FACC allowable maximum.

3.1.2 SWITCH AMPLIFIER CIRCUIT ANALYSIS

The switch amplifier employs deposited resistors, ceramic capacitors (ATC-111), and dual gate GaAs FETs. All parts are acceptably derated.

The voltage stresses for the capacitors range from 2% to 7% of rating. The temperature rise is less than 5° C.

The FETs are adequately derated:

Power	40%	versus	50% allowable
V_{DS}	50%	versus	75% allowable
V_{GS}	63%	versus	75% allowable
I_{DS}	30%	versus	90% allowable

The channel temperature for the FETs appears to be adequately derated and the temperature T is estimated to be between 30° C and 40° C. It seems that it should be possible to remain below 100° C overall channel temperature (FACC guidelines) for a flight design. The effects of incorporating temperature compensation are not known at this time in regards to possible increases in channel temperature.

3.2 DESIGN MODIFICATIONS FOR FLIGHT HARDWARE

The reliabiliy analyses which have been completed at this time have indicated that improvements will have to be made for actual flight hardware. These improvements are necessary to eliminate potential single piece part failure modes which could cause total failure of the matrix or unacceptable stress levels for individual parts. Recommended design improvements include the following:

1. There is concern that there is lack of feedback in the FET bias scheme to compensate for temperature drift and aging drift of the amplifiers. Even at beginning of life, a 25° C bias requires carefully selected resistor values to match gain characteristics between switches. Providing this compensation will require additional circuitry resulting in changes in component stresses and possible failure modes.

2. Additional levels of driver redundancy (possibly a doubling of

ICs and drivers) may be required to reduce potential single point driver failures.

3. Some failure modes in the switch driver and amplifier can result in +5V or -5V shorts. Such shorts could result in total switch matrix failure. Possible design improvements should be considered for an actual flight model.